# Lecture #33

## OUTLINE

- **IC Fabrication Technology**
  - – Doping
  - – Oxidation
  - – Thin-film deposition
  - – Lithography
  - – Etch

**<u>Reading</u>** (Rabaey *et al.*)

- Chapter 2.1-2.2

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# Integrated Circuit Fabrication

**Goal:**

Mass fabrication (*i.e.* simultaneous fabrication) of many "chips", each a circuit (e.g. a microprocessor or memory chip) containing millions or billions of transistors

**Method:**

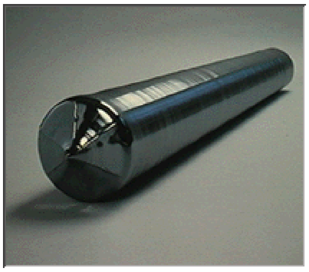
Lay down thin films of semiconductors, metals and insulators and pattern each layer with a process much like printing (lithography).

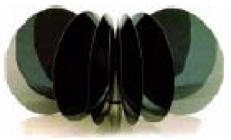
<u>Materials used in a basic CMOS integrated circuit:</u>

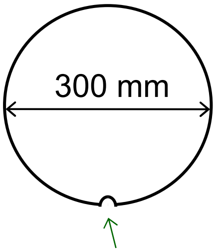
- Si substrate – selectively doped in various regions
- $SiO_2$ insulator
- Polycrystalline silicon – used for the gate electrodes
- Metal contacts and wiring

# Si Substrates (Wafers)

Crystals are grown from a melt in boules (cylinders) with specified dopant concentrations. They are ground perfectly round and oriented (a “flat” or “notch” is ground along the boule) and then sliced like baloney into wafers. The wafers are then polished.







**“notch” indicates crystal orientation**

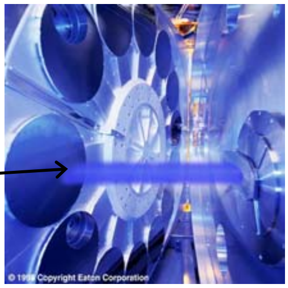
Typical wafer cost: $50

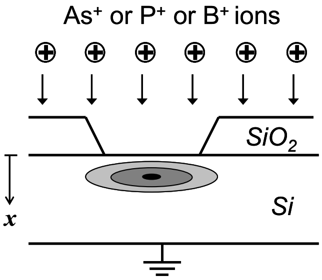
Sizes: 150 mm, 200 mm, 300 mm diameter

# Adding Dopants into Si

**Suppose we have a wafer of Si which is p-type and we want to change the surface to n-type. The way in which this is done by *ion implantation*. Dopant ions are shot out of an “ion gun” called an *ion implanter,* into the surface of the wafer.**

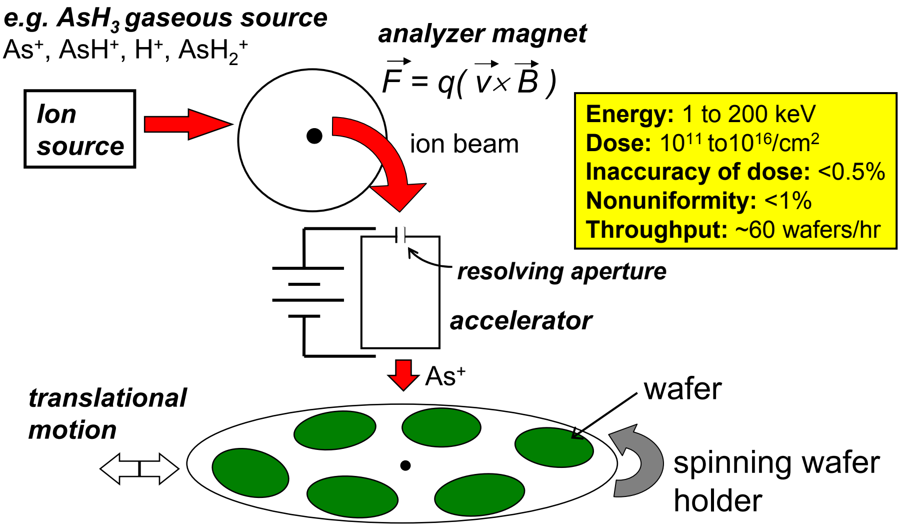
**Eaton HE3 High-Energy Implanter, showing the ion beam hitting the end-station**





**Typical implant energies are in the range 1-200 keV. After the ion implantation, the wafers are heated to a high temperature (~1000$^o$C). This “annealing” step heals the damage and causes the implanted dopant atoms to move into substitutional lattice sites.**

# Ion Implanter



**Energy:** 1 to 200 keV
**Dose:** $10^{11}$ to$10^{16}$/cm$^2$
**Inaccuracy of dose:** <0.5%
**Nonuniformity:** <1%
**Throughput:** ~60 wafers/hr

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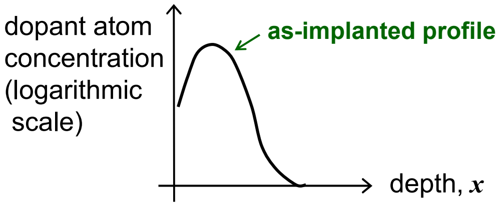
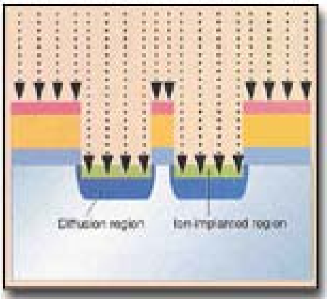
# Dopant Diffusion

- The implanted depth-profile of dopant atoms is peaked.





- In order to achieve a more uniform dopant profile, high-temperature annealing is used to diffuse the dopants
- Dopants can also be directly introduced into the surface of a wafer by diffusion (rather than by ion implantation) from a dopant-containing ambient or doped solid source

# Formation of Insulating Films

- **The favored insulator is pure silicon dioxide ($SiO_2$).**
- **A $SiO_2$ film can be formed by one of two methods:**
  1. **Oxidation of Si at high temperature in $O_2$ or steam ambient**
  2. **Deposition of a silicon dioxide film**

**ASM A412 batch oxidation furnace**

**Applied Materials low-pressure chemical-vapor deposition (CVD) chamber**

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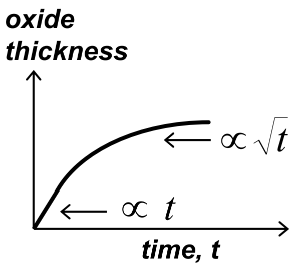
# Thermal Oxidation

$Si + O_2 \rightarrow SiO_2$ **or** $Si + 2H_2O \rightarrow SiO_2 + 2H_2$

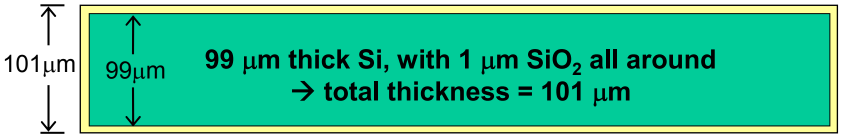
"dry" oxidation "wet" oxidation

- **Temperature range:**
  - 700°C to 1100°C
- **Process:**
  - $O_2$ or $H_2O$ diffuses through $SiO_2$ and reacts with Si at the interface to form more $SiO_2$
- **1 μm of $SiO_2$ formed consumes ~0.5 μm of Si**



# Example: Thermal Oxidation of Silicon

Thermal oxidation grows $SiO_2$ on Si, but it consumes Si, so the wafer gets thinner. Suppose we grow 1 μm of oxide:



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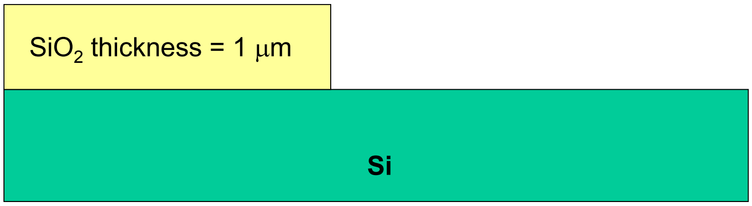
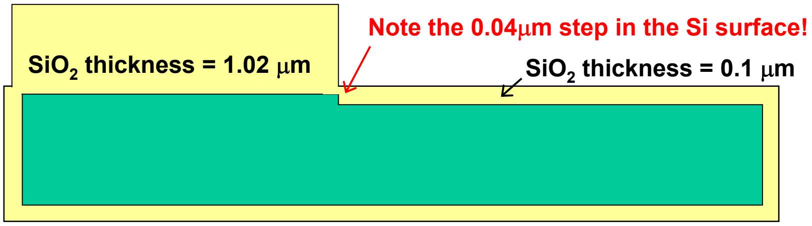
# Effect of Oxidation Rate Dependence on Thickness

- **The thermal oxidation rate slows with oxide thickness.**

  Consider a Si wafer with a patterned oxide layer:

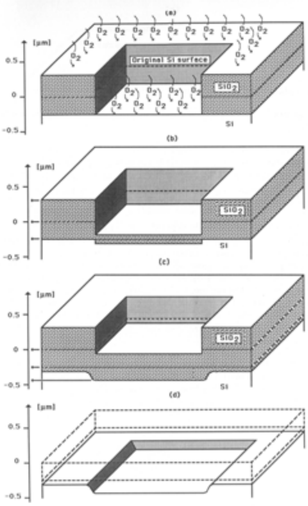


Now suppose we grow 0.1 μm of $SiO_2$:

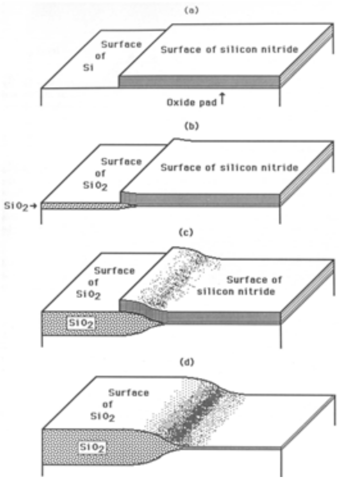


# Selective Oxidation Techniques

Window Oxidation



Local Oxidation (LOCOS)



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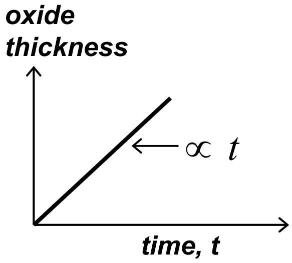
# Chemical Vapor Deposition (CVD) of $SiO_2$

$$\underset{\uparrow}{Si(C_2H_5O)_4} + 2H_2O \rightarrow SiO_2 + 4C_2H_6O$$

"TEOS" **or** $SiH_4 + O_2 \rightarrow SiO_2 + 2H_2$ "LTO"

- **Temperature range:**
  - 350$^o$C to 450$^o$C for silane
  - ~700$^o$C for TEOS
- **Process:**
  - Precursor gases dissociate at the wafer surface to form $SiO_2$
  - No Si on the wafer surface is consumed
- **Film thickness is controlled by the deposition time**



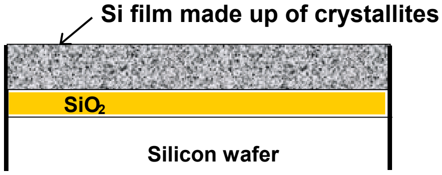
# Chemical Vapor Deposition (CVD) of Si

**Polycrystalline silicon** (“poly-Si”):

Like $SiO_2$, Si can be deposited by **C**hemical **V**apor **D**eposition:

- Wafer is heated to ~600°C
- Silicon-containing gas ($SiH_4$) is injected into the furnace:

$$SiH_4 \;=\; Si + 2H_2$$



**<u>Properties</u>:**

- **sheet resistance (heavily doped, 0.5 μm thick) = 20 Ω/□**
- **can withstand high-temperature anneals → major advantage**

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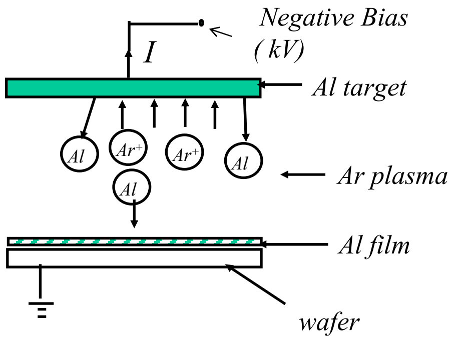
# Physical Vapor Deposition (“Sputtering”)

Used to deposit Al films:

Highly energetic argon ions batter the surface of a metal target, knocking atoms loose, which then land on the surface of the wafer

**Sometimes the substrate is heated, to ~300°C**



Gas pressure: 1 to 10 mTorr

Deposition rate $\propto I \bullet S$ ← sputtering yield

↖ ion current

# Patterning the Layers

Planar processing consists of a sequence of **additive** and **subtractive** steps with **lateral patterning**

↓ oxidation, deposition, ion implantation

↓ etching

↓ lithography

***Lithography*** refers to the process of transferring a pattern to the surface of the wafer

Equipment, materials, and processes needed**:**

- A mask (for each layer to be patterned) with the desired pattern
- A light-sensitive material (called ***photoresist***) covering the wafer so as to receive the pattern
- A light source and method of projecting the image of the mask onto the photoresist (“*printer*” or “*projection stepper*” or “*projection scanner*”)
- A method of “developing” the photoresist, that is selectively removing it from the regions where it was exposed

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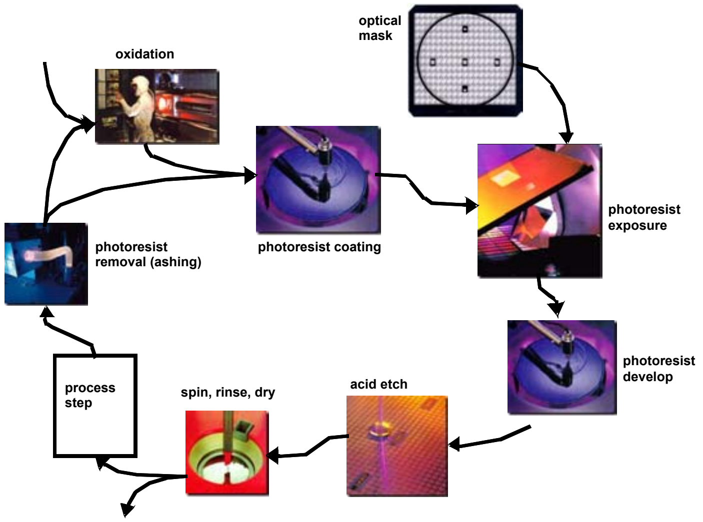
# The Photo-Lithographic Process



# Photoresist Exposure

- A glass mask with a black/clear pattern is used to expose a wafer coated with ~1 μm thick photoresist

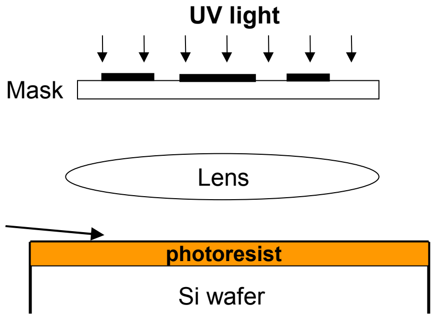


Image of mask appears here (3 dark areas, 4 light areas)

Mask image is demagnified by nX

“10X stepper”
“4X stepper”
“1X stepper”

Areas exposed to UV light are susceptible to chemical removal

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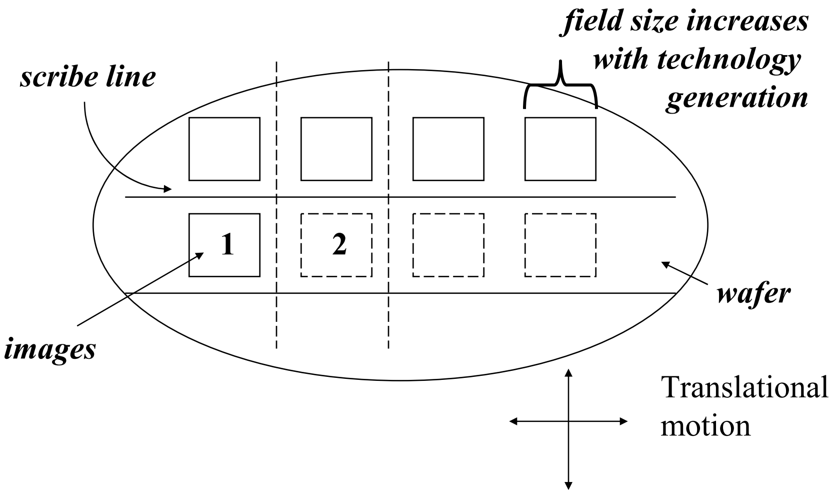
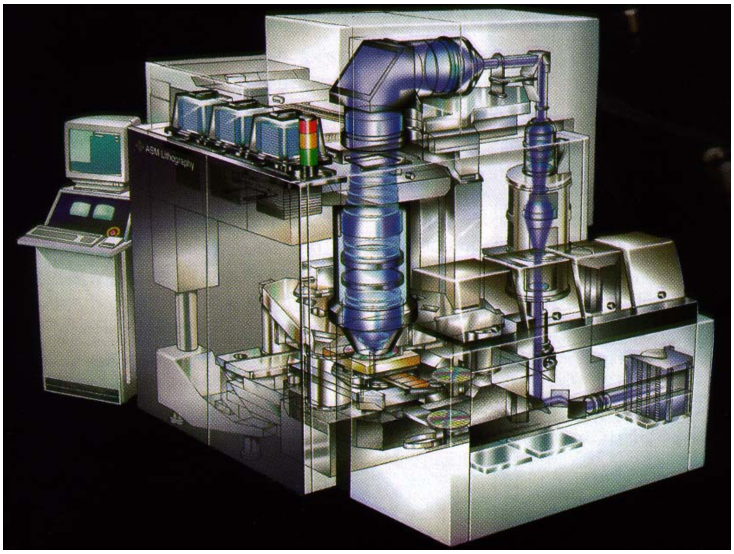
# Exposure using “Stepper” Tool



# Commercial Stepper Tool (ASM Lithography)



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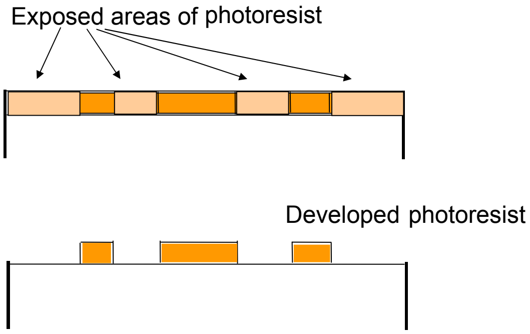
# Photoresist Development

- Solutions with high pH dissolve the areas which were exposed to UV light; unexposed areas are not dissolved



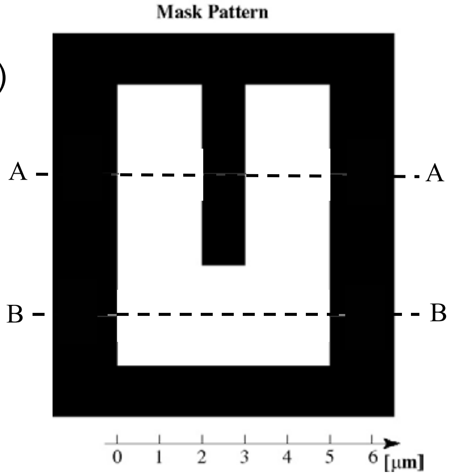
Exposed areas of photoresist

Developed photoresist

## Lithography Example

- Mask pattern (on glass plate)
- Look at cuts (cross sections) at various planes

  (*A-A* and *B-B*)



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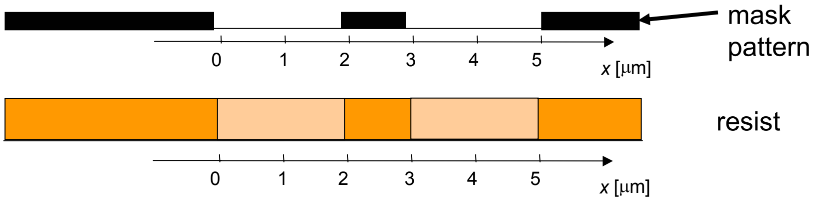
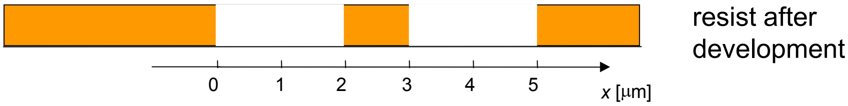
## “A-A” Cross-Section

**The resist is exposed in the ranges 0 < *x* < 2 μm & 3 < *x* < 5 μm:**

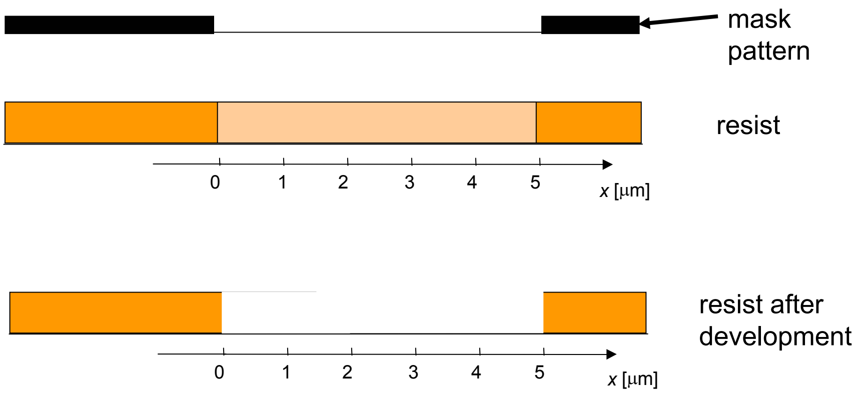


**The resist will dissolve in high pH solutions wherever it was exposed:**



# “B-B” Cross-Section

**The photoresist is exposed in the ranges $0 < x < 5$ μm:**



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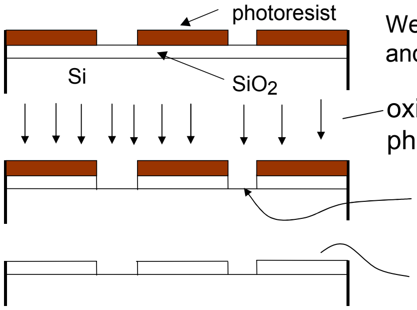
# Pattern Transfer by Etching

In order to transfer the photoresist pattern to an underlying film, we need a “subtractive” process that removes the film, ideally with minimal change in the pattern and with minimal removal of the underlying material(s)

→ **<u>Selective</u> etch processes (using plasma or aqueous chemistry) have been developed for most IC materials**



First: pattern photoresist

We have exposed mask pattern, and developed the resist

oxide etchant … photoresist is resistant.

Next: Etch oxide

etch stops on silicon (“**selective etchant**”)

Last: strip resist

only resist is attacked

**Jargon for this entire sequence of process steps: “pattern using XX mask”**