EE241B: Advanced Digital Circuits

Lecture 24 – Clocks

Time for course surveys!

Course Evaluations: Best Practices for Faculty

Reserve time in-class.
Give students time during class to complete the online course survey. Anecdotally, this is more effective when the time set aside is at the start of class.

Inform students about the purpose of evaluations.
Give students examples of useful feedback you have received in the past and how the course has changed or benefited.

Offer students incentives (e.g., extra credit).
To encourage broad, representative responses, instructors may choose to offer incentives to complete evaluations. An effective strategy has been to offer all students extra credit if a minimum percentage of students (e.g., 85%) respond.
Announcements

• Quiz today

• Final this Thursday, April 29, 9:40-11
  • In class, 80 min

• Project reports due on Wednesday, May 5, 9pm
  • Presentations on Thursday 9:30-11
Outline

• Digital PLLs
• Clocks and deskewing
• Supply droop mitigation
6.E Digital PLLs
Digital PLL

- Replace analog functions with digital equivalents

Digitally-controlled oscillator (DCO)
In IBM Power7 processor, per each core

Tierno, VLSI’10
6.F Deskewing and Synchronization
Clock Distribution

- Tree
- Mesh
- Grid
- H-Tree
- X-Tree
- Tapered H-Tree
Example Clock System

- IBM Power 4

Restle, ISSCC’02
Clock Grid

- Full-chip grid
- Tuned sector trees
- Buffer level 4 (64 Sector buffers)
- Buffer level 3
- Buffer level 2
- Buffer level 1
- Cloads

Delay (ps)

Time

X

Y
Clock Domain Synchronization

<table>
<thead>
<tr>
<th>Type</th>
<th>Frequency</th>
<th>Phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synchronous</td>
<td>Same</td>
<td>Same</td>
</tr>
<tr>
<td>Mesochronous</td>
<td>Same</td>
<td>Constant offset</td>
</tr>
<tr>
<td>Plesiochronous</td>
<td>Small difference</td>
<td>Slowly varying</td>
</tr>
<tr>
<td>Asynchronous</td>
<td>Different</td>
<td>Arbitrary</td>
</tr>
</tbody>
</table>
Deskew System (Mesochronous)
Clock Domain Crossings

- Bowhill, ISSCC’15
Brute-Force Synchronizer
Clock Crossing FIFOs

- FIFO for clock crossings

6.G Interaction Between Supply and Clock
Power Delivery

- Typical model

![Typical model diagram](image_url)

Wong, JSSC'06

EECS241B L25 SUPPLY
Supply Resonances

• First droop
  • Package L + on-die C

• Second droop
  • Motherboard + package decoupling

• Third droop
  • Board capacitors
What happens with supply?

http://www.research.ibm.com/people/r/restle/Animations/DAC01top.html
Clock and Supply

- Large digital systems can have large voltage transients
- Can we filter impact of voltage on a clock generator?

Kurd, JSSC’09
How to model

• Abstracted delay line

Period modulation from successive modulated delays

Wong, JSSC'06
• IBM Power7, with one PLL per core

Lefurgy, MICRO’11
Droop Detection

• Hashimoto, JSSC 4/18
Wrap-Up
This Class

• Put design choices in technology perspective

• The design constraints have changed and will be changing
  • Cost, energy, (power, leakage, …), performance

• Focused on variability, power-performance tradeoffs, power management

• Did not cover arithmetic, domino, I/O, supply generation, packaging, …
This Field

• Moore’s law will end sometime during your (my?) career
  • 5nm in 2021 scales to 0.1nm by 2050 with 2-yr cycles (or to 1nm with 5-yr cycles)

• Physics will stop CMOS somewhere ~2nm (?)
  • Will we see a different (CMOS) device in the meantime

• Economics will likely stop it somewhere while still in single digits
  • And the nodes will be stretched out

• We will see multi-chip/packaging solutions

• Don’t worry: Creativity is unlimited!
  • What can you build with 10B/100B/1 trillion transistors?
  • Even filling 10B-transistor chips with SRAM is not trivial!
This Field

• Focus on principles
• Watch out for opportunities
• Stay current!
Plan A: Extending Si CMOS

Plan B: Subsystem Integration

Plan C: Post Si CMOS Options

Plan Q: Quantum Computing

T.C. Chen, Where Si-CMOS is going: Trendy Hype vs. Real Technology, ISSCC'06