### Cerebras Unveils Wafer Scale Engine Two (WSE2): 2.6 Trillion Transistors, 100% Yield

By Dr. Ian Cutress on April 20, 2021.

<table>
<thead>
<tr>
<th>Feature</th>
<th>AnandTech</th>
<th>Wafer Scale Engine Gen1</th>
<th>Wafer Scale Engine Gen2</th>
<th>Increase</th>
</tr>
</thead>
<tbody>
<tr>
<td>AI Cores</td>
<td>400,000</td>
<td>850,000</td>
<td></td>
<td>2.13x</td>
</tr>
<tr>
<td>Manufacturing</td>
<td>TSMC 16nm</td>
<td>TSMC 7nm</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>Launch Date</td>
<td>August 2019</td>
<td>Q3 2021</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>Die Size</td>
<td>46,225 mm²</td>
<td>46,225 mm²</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>Transistors</td>
<td>1,200 billion</td>
<td>2,600 billion</td>
<td></td>
<td>2.17x</td>
</tr>
<tr>
<td>(Density)</td>
<td>25.96 mTr/mm²</td>
<td>56.246 mTr/mm²</td>
<td></td>
<td>2.17x</td>
</tr>
<tr>
<td>On-board SRAM</td>
<td>18 GB</td>
<td>40 GB</td>
<td></td>
<td>2.22x</td>
</tr>
<tr>
<td>Memory Bandwidth</td>
<td>9 PB/s</td>
<td>20 PB/s</td>
<td></td>
<td>2.22x</td>
</tr>
<tr>
<td>Fabric Bandwidth</td>
<td>100 Pb/s</td>
<td>220 Pb/s</td>
<td></td>
<td>2.22x</td>
</tr>
<tr>
<td>Cost</td>
<td>$2 million+</td>
<td>arm+leg</td>
<td></td>
<td>?</td>
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</table>
Announcements

• Assignment 4 due this Friday
  • Quiz next Tuesday

• Final next Thursday, April 29, 9:40-11
  • In class, 80 min

• Project reports due on Wednesday, May 5, 9pm
  • Presentations on Thursday 9:30-11
Outline

• Optimal thresholds and supplies
• Clock generation
6.C Clock Generation: PLLs
Phase-Locked Loop

- PLL is locked when the phase difference is zero
- Second/third order loop
- ÷N for frequency synthesis (and x M)
- Filters input jitter
- Accumulates phase error
Voltage-Controlled Oscillator

- Oscillation frequency controlled by voltage

\[ \omega_{out} = \omega_{FR} + K_{VCO} V_{ctrl} \]

\[ y_{out}(t) = A \cos \left( \omega_{FR} t + K_{VCO} \int_{-\infty}^{t} V_{ctrl} dt \right) \]

\( \omega_{FR} \) – free-running frequency
Example VCO

• Ring-oscillator-based VCO: RC loaded

➤ Ring-oscillator-based VCO: Current-starved
PLL vs. DLL Dynamics

• The key difference is in the VCDL vs. VCO transfer characteristics

• VCO integrates (accumulates) phase

\[ H_{VCO}(s) = \frac{K_{VCO}}{s} \]
Charge Pump

• Push/pull current source operation
Charge-Pump PLL

Phase transfer function

\[
H(s) = \frac{K_{PFD} \cdot K_{VCO}}{\frac{1}{s} + \frac{K_{PFD}}{s} \cdot \frac{1}{s}} = \frac{K_{PFD}K_{VCO}}{s^2 + K_{PFD}K_{VCO}}
\]
Charge Pump PLL with a Zero

- Charge pump PLL has a stability problem
- Compensation by adding a zero
Charge Pump PLL with a Zero

\[ H(s) = \frac{K_{VCO} \cdot I}{2\pi C_P} \cdot \frac{1}{s^2 + \frac{I}{2\pi} K_{VCO} R_S + \frac{I}{2\pi C_P} K_{VCO}} \]

\[ \omega_n = \sqrt{\frac{I}{2\pi C_P} K_{VCO}} \]

\[ \zeta = \frac{R}{2} \sqrt{\frac{I C_P}{2\pi} K_{VCO}} \]
Higher Order Loops

• Another pole naturally exists
  • Filters the control voltage $V_{CTRL}$
  • Lowers phase margin
  • Reduces the lock range $V_{DD}$
Phase Noise at the PLL Input

- Low-pass characteristic

\[ H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \]

\[ |\log \Phi_{out}/\Phi_{in}| \]
VCO Phase Noise

- High-pass characteristic

\[
\Phi_{out}(s) = \frac{s(s + \omega_{LPF})}{s^2 + 2\zeta\omega_n s + \omega_n^2}
\]

\[
|\log\frac{\Phi_{out}}{\Phi_{VCO}}(s)|
\]

\[
\omega
\]
6.D Supply Generation
Supply Generation

• Linear
  • Series or shunt
  • Linear regulation
  • Quiet
  • Inefficient (unless Vin-Vout is small)

• Switching (Capacitive)
  • Limited efficiency
  • Poor regulation
  • Voltage ripples

• Switching (Magnetic)
  • Efficient
  • Require external components
  • Noisy
Linear vs. Switching Regulators
Linear Voltage Regulator
Switching Supply
Inside Haswell

Integrated VR Technology

- 'Common Cell' Architecture – 20 cells
- Architecture supports flat efficiency curve
- Fine grain power management
  - Allows for multiple voltage rails
- Telemetry and Margining features
- Active Voltage Positioning for current sharing and balance
- Control features, including: JTAG, FPGA, Test/BIST

Power cell
- 2.8 mm²
Inside Haswell

Review: Power Cell Architecture

- Each Power cell = Mini VR
  - Up to 25A rating* - tested
  - Programmable switching frequency
    30MHz to 140MHz
  - Ring coupled inductor topology

- 16 phases per power cell, 320 phases per chip
  - High phase count reduces noise, ripple
  - High granularity
  - Cell shedding
  - Bridge shedding

- BIST
  - Self-load and characterization system.

* Thermally constrained
**Intel Broadwell**

- Inductors moved to a small PCB
Switched-Capacitor Supply
Next Lecture

• Optimal supplies and thresholds
• Clocking