Spending $50B on the Chip Industry is a Challenge, EETimes
Chip industry executives have a huge collective challenge: deciding how to prioritize the $50 billion in support promised by President Joseph R. Biden in an executive order.
Semiconductor industry executives met virtually with President Biden to discuss the issues around chip capacity and supply chain. Neither the Semiconductor Industry Association (SIA) nor the White House readouts of the meeting told us anything new. The President did acknowledge however that the $50 billion support package is not likely to be enough, stating, “We are seeking a significant investment in this piece of legislation. It’s important, but we know it’s not sufficient.”

Announcements
• Assignment 4 due this Friday
  • Quiz next Tuesday
• Final next Thursday, April 29, 9:40-11
  • In class, 80 min
• Project reports due on Monday, May 3, 9am
  • Presentations on Monday afternoon

May 6

Abstract
1. Introduction
2. Background
3. Your solution
4. Experimental setup
5. Results
6. Conclusion
References
Outline

• Optimal thresholds and supplies
• Clock generation

5.0 Optimal $V_{DD}$, $V_{Th}$
Dynamic Voltage Scaled Microprocessor

External $V_{DD}$: 3.3V ±10%
Internal $V_{DDL}$: 0.8V~2.9V ±5%

Adapting $V_{DD}$ and $V_{TH}$

- Adapting both $V_{DD}$ and $V_{TH}$ during runtime
  - $V_{TH}$ is much less sensitive

Miyazaki, ISSCC’02

Courtesies: Prof. Kuroda
Adapting $V_{DD}$ and $V_{TH}$

- Adjusting $V_{DD}$, $V_{TH}$ trades off energy and delay
- We studied energy-limited design
  - And alternate ways for optimizing energy and delay together
  - E.g. energy-delay product (EDP)
  - Or $E^nD^m$, $n,m > 1$

Miyazaki, ISSCC’02
Optimal EDP Contours

- Plot of EDP curves in $V_{DD}$, $V_{TH}$ plane

![Graph showing EDP contours in $V_{DD}$, $V_{TH}$ plane](image)

$\sigma^2 + P_L t$

Gonzalez, JSSC 8/97

Technology parameters ($V_{dd}^{max}$, $V_{th}^{ref}$) rarely optimal:

- Large variation in optimal circuit parameters $V_{dd}^{opt}$, $V_{th}^{opt}$, $w^{opt}$

Sizing, Supply, Threshold Optimization

<table>
<thead>
<tr>
<th>Topology</th>
<th>Inverter</th>
<th>Adder</th>
<th>Decoder</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>($E_L/E_{Sw}^{ref}$)</td>
<td>0.1%</td>
<td>1%</td>
</tr>
</tbody>
</table>

Reference Design:

$D^{ref} (V_{dd}^{max}, V_{th}^{ref})$

Large variation in optimal circuit parameters $V_{dd}^{opt}$, $V_{th}^{opt}$, $w^{opt}$
Result: E-D Tradeoff in an Adder

Energy efficient curve $f(W,Vdd,Vth)$

Delay (Dref)

Reference Design $(D_{ref},E_{ref})$

Energy (E_{ref})

Sensitivity

\begin{array}{|c|c|c|}
\hline
\text{Sensitivity} & W & Vdd & Vth \\
\hline
(D_{ref},E_{ref}) & \infty & 1.5 & 0.2 \\
(D_{min},E_{ref}) & 1 & & \\
(D_{min},E_{min}) & 22 & 16 & 22 \\
\hline
\end{array}

80% of energy saved without delay penalty

40% delay improvement without energy penalty

Energy-constrained delay

- Active power
  \[ P_{act} = \alpha fCV_{DD}^2 \]
  \[ f = 1/L_{Dp} \]

- Leakage power
  \[ P_{leak} = I_0 e^{-V_{th} - \gamma V_{DD}} \]

- Eliminate one variable ($V_{th}$) and find $P_{min}(V_{DD})$

Nose, ASP-DAC'00
Minimum energy: $E_{Sw} = 2E_{Lk}$

- Large $(E_{Lk}/E_{Sw})^{opt}$
- Flat $E_{Op}$ minimum
- Topology dependent

$$\frac{E_{Lk}}{E_{Sw}}^{opt} = \frac{2}{\ln \left( \frac{L_d}{\alpha_{avg}} \right) - K}$$

Optimal designs have high leakage $(E_{Lk}/E_{Sw} \approx 0.5)$

Subthreshold Optimum

$f = 30\,kHz$

Minimum is independent of $V_T$
6. Clocks and Supplies

Clock Subsystem

- Clock Generation
- Clock Distribution
- Synchronization
Clock Subsystem

• Intel Xeon – Bowhill, ISSCC’15
  • Independent clocks for 4-18 cores
• Self-biased (SB) and LC PLLs

6.B Clock Generation
Clock Generation

Delay-Locked Loop (Delay Line Based)

Phase-Locked Loop (VCO/DCO-Based)

PLL Signals
Loop Performance

- Ideal clock
- Clock with jitter
- Phase offset, peak-to-peak jitter, RMS jitter
- Bandwidth, locking time, frequency range

Phase Detector

- Detects the phase difference

\[ V_{\text{out}} = K_{\text{PD}} \cdot \Delta \phi \]
Delay-Locked Loop

- First order loop: inherently stable
- No filtering of input jitter
- Constant frequency (no synthesis)
- No phase error accumulation

DLL Locking

Delay-Locked Loop

- Open loop transfer function
  \[ \frac{D_0(s)}{D_1(s) - D_0(s)} = K_{PD} \frac{I_{CP}K_FF_{REF}}{sC} = \frac{1}{s}K_{PD}K_FK_{DL} \]

- Closed loop transfer function
  \[ H(s) = \frac{D_0(s)}{D_1(s)} = \frac{K_{PD}K_FK_{DL}}{s + K_{PD}K_FK_{DL}} \]

- \( \omega_N > \) an order of magnitude below \( F_{REF} \)
- Use of DLLs requires low-jitter input
- VCDL must span adequate delay range + reset to min delay
- Noise sources:
  - Delay line (Supply sensitivity)
  - Clock buffers that follow
  - Device noise (small)
Voltage-Controlled Delay Line

- Delay controlled by voltage with proportionality $K_{DL}$

DLL Uses
Next Lecture

• PLLs
• Clock distribution