EE241B : Advanced Digital Circuits

Lecture 15 – SRAM

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https://beagleboard.org/beaglev
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SPECIFICATIONS
Processor
- RISC-V U74 Dual core with 2MB L2 cache @ 1.0GHz
- Vision DSP Tensilica-VP6 for computing vision
- NVDLA Engine 1 core (configuration 2048 MACs@800MHz)
- Neural Network Engine (1024MACs@500MHz)
Memory
- 8GB LPDDR4 (2 x 4GB LPDDR4 SDRAM)
Video Processing
- Video Decoder (H264/H265) up to 4K@60FPS; Support Dual stream decoding for 2K@30FPS
- Dual channels of ISP, each channel support up to 4K@30FPS
- 2 x MIPI-CSI, 1 x MIPI-DSI
- 1 x HDMI 1.4 support up to 1080P@60fps
- Support MIPI-CSI TX for video output after ISP and AI processing
- JPEG encoder/decoder
Announcements

• Quiz today
  • 15 minutes 11am-7pm

• Create webpages (github) for your projects!
  • And e-mail me the links!!

• Midterm reports due this week

• Lab 4 due this week
Outline

• **SRAM**
  • Static and dynamic margins
4. Memory
4.B SRAM Static Retention Margin
6T-SRAM Array Basics – Write Operation

- BLT discharged to GND by Write Driver
- High-node discharged through series stacked NFET devices. NFET effective device strength must overcome cell pull-up.
- “Weak” 1 written through source-follower NFET x-fer device
6T-SRAM Array Basics – Read Operation

Local Read Circuit

Sense Amplifier: Longer BLs

Domino: Short BLs, SOI

Positive feedback causes high-node to droop

Pull-down / Transfer-device ratio (Beta ratio) determines how high the low node rises
Scaling trend:

- Increased gate leakage + degraded $I_{ON}/I_{OFF}$ ratio
- Lower $V_{DD}$ during standby

PMOS load devices must compensate for leakage.
Retention Stability

- Would like to reduce supply in standby

Retention SNM @ 0.6V
Retention SNM @ 1V
Monte-Carlo Simulation of DRV Distribution

 DRV – Data retention voltage

Histogram of cell #

Simulated DRV of 1500 SRAM cells (mV)

Qin, ISQED’04
Vmin Distribution

• Aggregate minimum operating voltage
• Digital test under supply sweep
4.C Static Read/Write Margins
• Read SNM is the contention between the two sides of the cell under read stress.

\[ \Delta V_{Th} \propto \frac{1}{C_{ox} \sqrt{WL}} \]  

Due to RDF

E. Seevinck, JSSC 1987
Read SNM - Measurements

Read margin vs. retention margin

Bhavnagarwala, IEDM’05
Write Stability – Write Noise Margin (WNM)

- Writeability is becoming harder with scaling
- Optimizing read stability and writeability at the same time is difficult
Writeability – BL/WL Write Margins

- Highest BL voltage under which write is possible when BLC is kept precharged
- Difference between VDD and lowest WL voltage under which write is possible
Write Stability – Write Current (N-Curve)

- Minimum current into the storage node

C. Wann et al, IEEE VLSI-TSA 2005
The Conflict Between Read and Write

READ - OPTIMIZED SYSTEM

WRITE - OPTIMIZED SYSTEM

LARGE

SMALL

Large Beta (Tpd/Tpg)

Large Gamma (Tpu/Tpg)

Small Beta (Tpd/Tpg)

Small Gamma (Tpu/Tpg)

Write Driver

Sense Amplifier

Write Driver

Sense Amplifier
V_{Th} Window

- Assuming global spread

![Diagram showing V_{Th} window for pMOS and nMOS with read and write limits for different process nodes.]

Yamaoka, ISSCC’05
4.D Dynamic Margins
6-T SRAM Static/Dynamic Stability

- **Read Margin**
  - SNM: pessimistic

- **Write Margin**
  - WNM: optimistic

- **Introduction to dynamic margins**
  - Three failure modes: read stability, writeability and read access time
Dynamic Write Stability

- $T_A < T_{\text{write}} < T_B$
- $T_{\text{write}} =$ dynamic write stability
- Static margins are optimistic

Khalil, TVLSI′08
Dynamic Read Stability

TA < T_{read} < TB

T_{read} = \text{dynamic read stability}

Static margins are pessimistic

Khalil, TVLSI ‘08
Dynamic Read Access

- $T_A < T_{\text{access}} < T_B$
- $PD_1$ and $PG_1$ are critical

Khalil, TVLSI '08
SRAM Overall $V_{min}$

- Both read and write
- Some contradicting data
SRAM Vmin Scaling Trend

- SRAM voltage often higher than logic

![Graph showing SRAM Vmin scaling trend across different node sizes with write assist indicated.]

- J. Chang, ISSCC'20
4.E SRAM Peripheral Circuits
Peripheral Circuits in SRAM

• Decoders (and pre-decoders)
• Column circuitry: read, write, multiplex, mask
• Write assist techniques
• Read assist techniques
• Redundancy
• BIST
• ECC
• Power management
SRAM Array
Next Lecture

- SRAM guest lecture