EE241B : Advanced Digital Circuits

Lecture 14 – Memory

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Xilinx Opens Up Vitis HLS Tool for FPGAs
By Kevin Krewell 03.09.2021 EETimes

Open sourcing software that was previously proprietary is a great way to expand community engagement and encourage more innovation. Xilinx posted the code on the GitHub repository opening the code for the community to use. Xilinx will release future versions to GitHub as well. [Vitis HLS LLVM GitHub Repository]

Announcements

• Assignment 2 due this week
  • Followed by a quiz next Tuesday

• Create webpages (github) for your projects!
  • And e-mail me the links!

• Midterm reports due next week
Outline

• Pulse-triggered flip-flops
• Introduction to SRAM

3. Design for Performance

3.F Flip-Flops
Intel/HP Itanium 2

Naffziger, ISSCC’02

Pulsed Latches

Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC’96
Pulsed Latches

7474, from mid-1960's

First stage is a sense amplifier, precharged to high, when $Clk = 0$
After rising edge of the clock sense amplifier generates the pulse on $S$ or $R$
The pulse is captured in S-R latch
Cross-coupled NAND has different propagation delays of rising and falling edges

DEC Alpha 21264, StrongARM 110
Sampling Window Comparison

Naffziger, JSSC 11/02
4. Memory

Random Access Memory Architecture

• Conceptual: Linear array of addresses
  • Each box holds some data
  • Not practical to physically realize
    – millions of 32b/64b words

• Create a 2-D array
  • Decode Row and Column address to get data
Basic Memory Array (From 151/251A)

- Core
  - Wordlines to access rows
  - Bitlines to access columns
  - Data multiplexed onto columns
- Decoders
  - Addresses are binary
  - Row/column MUXes are ‘one-hot’ - only one is active at a time

Memory Banks

- Traditionally addressed by the LSB
  - Example two-bank memory
  - Odd and even banks

0xFFFF...F 0xFFFF...E
0xFFF...F 0xFFF...E
0x000...F 0x000...E
0x000...1 0x000...0
SRAM Cell Trends

SRAM Scaling or Not?

• TSMC at IEDM’19

• Bora’s spreadsheet

• TSMC at ISSCC’20
SRAM Topics

A. Basics and trends
B. Static retention margin
   C. Static read/write margins
D. Dynamic margins
D. Assist techniques
E. Periphery, redundancy and error correction
F. Scaling options

4. Memory
   4.A SRAM Basics and Trends
6-T SRAM Cell

- Improve CD control by unidirectional poly
- Special SRAM design rules

SRAM Cell Design Trends

- Key enabling technology: STI
- Impact:
SRAM Cell Trends (22nm)

0.092μm² cell in 22nm from Intel (IDF'09)

A little analysis by using a ruler:
- Aspect ratio 2.9
- Height \(\sim\) 178nm, Width \(\sim\) 518nm
- Gate \(\sim\) 45nm (Lg is smaller)

0.346μm² cell in 45nm from Intel (IEDM'07)

22nm SRAM – Discrete Widths

- FinFET cell design

1:1:1
N:N:P

E. Karl, ISSCC'12
14nm SRAM

- Aspect ratio ~ 2.5
- Cell area = 0.05um²
  - Height = 140nm (2 gate p)
  - Width = 350nm
  - Lg ~ 32nm

E. Karl, ISSCC’15

10nm SRAM

- HDC 1:1:1
- LVC 1:1:2

Guo, ISSCC’18
4. Memory

4.B SRAM Static Retention Margin
SRAM Cell/Array

- Hold (retention) stability
- Read stability
- Write stability
- Read access time

Access Transistor

Pull down
Pull up

SRAM Operation

Write

Retention

Read