EE241B : Advanced Digital Circuits

Lecture 12 – Latches

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The long road
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Science 19 Feb 2021:
Vol. 371, Issue 6531, pp. 768-772

Early signs suggest COVID-19 vaccines are having an impact, but questions abound about the path to normal.

Announcements
• Labs 3 due this week
• Assignment 2 due next week
  • Followed by a quiz
• Create webpages (github) for your projects!
Outline

- Latch-based timing
- Latch design

3.C Latch Timing
**Key Point**

- Latch-based sequencing can improve performance, but is more complicated
  - Timing analysis not limited to a consecutive pair of latches

**Latch Timing**

- When data arrives to transparent latch: 
  - Latch is a ‘soft’ barrier
- When data arrives to non-transparent latch: 
  - Data has to be ‘re-launched’
Latch Sequencing

1) 

[Diagram showing two latches with clock inputs and logic]

2) 

[Diagram showing two latches with clock inputs and logic]

Preventing Late Arrivals

1) 

[Diagram showing two latches with clock inputs and logic]

- Early RAT
- Late RAT
- Data can launch during transparency

Arrives to early transport path

Arrives to late transport path

\[ T_{cw} + T_{lm} + T_{su} < 1.5 T_{co} \]
Preventing Premature Arrivals

- Data should not be able to race through during transparency

Two-Phase Latch-Based Design

- Two-phase non-overlapping is safer, but adds margin
Latch-Based Timing

• Single-phase, two-latch

As long as transitions are within the assertion period of the latch, no impact of position of clock edges.
Soft-Edge Properties of Latches

- **Slack passing** – logical partition uses left over time (slack) from the previous partition
- **Time borrowing** – logical partition utilizes a portion of time allotted to the next partition
- Makes most impact in unbalanced pipelines

Bernstein et al, Chapter 8, Chandrakasan, Chap 11 (by Partovi)
Slack Passing and Time Borrowing

• Slack passed

Slack Passing and Time Borrowing

• Time borrowed
Slack-Passing and Cycle Borrowing

For N stage pipeline, overall logic delay should be < N TcL

3. Design for Performance

3.D Latch Design

Skew = max deviation between two clock endpoints
Review: MUX

- 2-input MUX

\[ Y = \begin{cases} A & \text{if } \text{Sel} = 1 \\ B & \text{if } \text{Sel} = 0 \end{cases} \]

Review: Transmission Gates

- Transmission Gates (HL, LH)

\[ R = \begin{cases} \frac{R}{2R} & \text{for } \text{HL} \\ \frac{2R}{R} & \text{for } \text{LH} \end{cases} \]

\[ R = \frac{2}{3} R \]
Generating Complementary Clocks

\[ d_1 = \frac{1 + \frac{c_1}{c_2}}{c_1 + c_2} = \frac{c_1}{c} \]
\[ d_2 = \frac{2 + 2 \sqrt{\frac{c_1}{c}}}{C - c_1} = 2 + 2 \sqrt{\frac{c_1}{c}} \]
\[ \frac{c_L}{c} = \Phi \]

\[ g_{inv. dark} \approx 1 \]

Latch vs. Flip-Flop

(a) Latch

(b) Flip-flop

Latches

Transmission-Gate Latch

Usually without contention

C²MOS Latch

Latches

(a) The transparent high latch (THL)
(b) The transparent low latch (TLL)

(c) Timing waveforms for the THL

3. Design for Performance

3. E Delay, Setup, Hold

Latch $t_{D-Q}$ and $t_{Clk-Q}$

\[
F = 1
\]

\[
t_{D-Q} = (g_1 h_1 + p_1 + g_2 h_2 + p_2) t_{w+} = (1.2 + 1.5 + 1.2 + 1) t_{w+} = 4.9 t_{w+} \approx 1 \text{ Fo4}
\]

\[
g_1 h_1 = g_2 h_2 = \sqrt{1.5} = 1.2
\]

\[
L = g_1, g_2 = 1.5
\]

\[
F = 1
\]

\[
\]

\[
t_{Clk-Q} \approx 4.9 t_{w+} \approx 1 \text{ Fo4}
\]

\[
G = G_1, G_2 = 1.5
\]

\[
F = 1
\]

\[
\]

\[
\]