ISSCC'21 Papers

M. Liu, Keynote

H. Chen, Processors
Announcements

• Assignment 1 + Lab 2 due next week
• No lecture next Tuesday
Outline

• Leakage
• C-V models
• Gate delays
2.F Transistor Leakage
Transistor Leakage
Transistor Leakage

Leakage current is exponential with $V_{GS}$.

$V_{DS} = 1$V

Subthreshold slope
Transistor Leakage (130nm)

Two effects:
- diffusion current (like a bipolar transistor)
- exponential increase with $V_{DS}$ (DIBL)
Transistor Leakage (32nm LP PTM)

Another view of DIBL

>10x increase in leakage

$I_{\text{Leak}}$ [A]

$V_{DS}$ [V]
Subthreshold Current

- Subthreshold behavior can be modeled physically

\[
I_{ds, subth} = \mu_{eff} C_{ox} \frac{W}{L} (m - 1) \left( \frac{kT}{q} \right)^2 e^{\frac{V_{GS} - V_{Th}}{mkT/q}} \left( 1 - e^{\frac{V_{ds}}{kT/q}} \right)
\]

\[
m = 1 + \frac{C_{dm}}{C_{ox}} \quad (m \sim 1.1-1.4)
\]

Or (approx):

\[
I_{ds, subth} = I_0 \frac{W}{W_0} 10^{\frac{(V_{gs} - V_{th}) + \gamma V_{ds}}{S}}
\]

\[
S = 2.3m \frac{kT}{q}
\]

Taur, Ning, Modern VLSI Devices
Leakage Components

![Image of leakage components diagram](image-url)

Source $n^+$ $I_2$ $I_3$ $I_6$ $I_5$

Gate $I_7$ $I_8$

Drain $n^+$ $I_1$

Well $p$-well $I_4$

Leakage Components (250nm)

1. pn junction reverse bias current
2. Weak inversion
3. Drain-induced barrier lowering (DIBL)
4. Gate-induced drain leakage (GIDL)
5. Punchthrough
6. Narrow width effect
7. Gate oxide tunneling
8. Hot carrier injection

Leakage ($I_{OFF}$) Current in Amps

- $1E-7$: weak inversion + p-n junction + DIBL + GIDL @ $V_D = 3.9V$
- $1E-8$: weak inversion + p-n junction + DIBL @ $V_D = 2.7V$
- $1E-9$: weak inversion + p-n junction (80 mV/dec & $V_D = 0.1V$)
- $1E-10$: p-n junction
- $1E-11$
- $1E-12$
- $1E-13$

1. No punchthrough
2. No width effect
3. No gate leakage
Leakage Components

• Drain-induced barrier lowering (DIBL)
  • Voltage at the drain lowers the source potential barrier
  • Lowers $V_{Th}$, no change on $S$

• Gate-induced drain leakage (GIDL)
  • High field between gate and drain increases injection of carriers into substrate -> leakage
    (band-to-band leakage)
2.H Transistor C-V
MOS Transistor as a Switch

Discharging a capacitor

• Can solve:
  
  \[
  i_{DS} = i_{DS}(v_{DS})
  \]
  
  \[
  i_{DS} = C(v_{DS}) \frac{dv_{DS}}{dt}
  \]

• Prefer using equivalent resistances
• Find \( t_{pHL} \)
• Find equivalent C, R
MOS Capacitances

• Gate capacitance
  • Non-linear channel capacitance
  • Linear overlap, fringing capacitances
  • Miller effect on overlap, fringing capacitance

• Non-linear drain diffusion capacitance
  • PN junction

• Wiring capacitances
  • Linear
Gate and Drain Capacitances

Gate capacitance

Drain capacitance
Gate Capacitances
Gate Capacitances

• Gate capacitance is non-linear
  • First order approximation with $C_{ox}WL$ ($C_{ox}L = 2fF/\mu m$)

• Need to find the actual equivalent capacitance by simulating it

• Since this is a linear approximation of non-linear function, it is valid only over the certain range
  • Different capacitances for HL, LH transitions and power computation

• Drain capacitance non-linearity compensates
  • But this changes with fanout
2.1 Delay Revisited
MOS Transistor as a Switch (EECS251A)

\[ R_{eq} = \text{average}_{t = t_1 \ldots t_2}(R_{on}(t)) = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} R_{on}(t) dt = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} \frac{V_{DS}(t)}{I_D(t)} dt \]

\[ \approx \frac{1}{2}(R_{on}(t_1) + R_{on}(t_2)) \]
Solving the integral:

\[ R_{eq} = \frac{1}{-V_{DD}/2} \int_{V_{DD}}^{V_{DD}/2} \frac{V}{I_{DSAT}(1 + \lambda V)} dV \approx \frac{3}{4I_{DSAT}} \frac{V_{DD}}{(1 - \frac{7}{9} \lambda V_{DD})} \]

with appropriately calculated \( I_{dsat} \)

Averaging resistances:

\[ R_{eq} = \frac{1}{2} \left( \frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)} \right) = \frac{3}{4I_{DSAT}} \left( 1 - \frac{5}{6} \lambda V_{DD} \right) \]
CMOS Performance

Propagation delay: \[ t_{pHL} = (\ln 2)R_{eqn}C_L \quad t_{pLH} = (\ln 2)R_{eqp}C_L \]

\( \ln 2 = 0.7 \)
Switching Trajectory

V_{DS}[V]

I_{DS}[A]
Effective Current

- $I_{on}(V_{DD})$ is never reached
- Define $I_{eff} = (I_H + I_L)/2$
- $I_L = I_{DS}(V_{GS}=V_{DD}/2, V_{DS}=V_{DD}); I_H = I_{DS}(V_{GS}=V_{DD}, V_{DS}=V_{DD}/2)$
DIBL Matters

- A. Loke, VLSI’16

FinFET, FDSOI – less DIBL

\[ L_{\text{eff}} = \frac{L_{\text{LO}} + L_{\text{HI}}}{2} \]

\[ L_{\text{LO}} @ V_{GS} = \frac{1}{2} V_{DD}, \ V_{DS} = V_{DD} \]

\[ L_{\text{HI}} @ V_{GS} = V_{DD}, \ V_{DS} = \frac{1}{2} V_{DD} \]

\( L_{\text{eff}} \) is better than \( L_{\text{Dsat}} \) for estimating inverter CV/I switching delay

Less DIBL \( \rightarrow \) higher \( L_{\text{eff}} \) & \( r_{\text{out}} \) for same \( L_{\text{Dsat}} \)
Transistor Stacks

![Graph showing the relationship between V_DS and I_DS for different values of V_DS.](image-url)
Effective Current in Stacks

- Add linear current, $I_3$

\[
\begin{array}{c|c|c|c|c}
V_{dd} & V_{dd}/2 & V_{dd} & V_{dd}/2 & V_{dd} \\
\hline
V_{gs} & V_{gs}/2 & V_{gs} & V_{gs}/2 & V_{gs} \\
\hline
0.05V & 0.05V & 0.05V & 0.05V & 0.05V \\
\end{array}
\]

Model:
\[I_{\text{stack1}} = c_{H1}I_H + c_{L1}I_L + c_{31}I_3 \]

Inverter:
\[I_{\text{stack1}} = 0.45I_H + 0.48I_L + 0.07I_3 \]
NAND2/NOR2:
\[I_{\text{stack2}} = 0.18I_H + 0.38I_L + 0.44I_3 \]
NAND3/NOR3:
\[I_{\text{stack3}} = 0.08I_H + 0.36I_L + 0.56I_3 \]

Von Arnim, IEDM'2007
Next Lecture

- Standard cells, design kit