Announcements

• Assignment 1 + Lab 2 due next week
• No lecture next Tuesday
2. F Transistor Leakage
Transistor Leakage

Leakage current is exponential with $V_{GS}$.

Subthreshold slope

$V_{DS} = 1V$
Transistor Leakage (130nm)

Two effects:
- diffusion current (like a bipolar transistor)
- exponential increase with $V_{DS}$ (DIBL)

Transistor Leakage (32nm LP PTM)

Another view of DIBL
>10x increase in leakage
Subthreshold Current

- Subthreshold behavior can be modeled physically

\[
I_{ds,\text{subth}} = \mu_{\text{eff}} C_{\text{ox}} \frac{W}{L} (m-1) \left( \frac{kT}{q} \right)^2 e^{\frac{V_{GS}-V_{TH}}{m kT/q}} \left( 1 - \frac{V_{DS}}{kT/q} \right)
\]

\[
m = 1 + \frac{C_{dm}}{C_{ox}} \quad (m \sim 1.1-1.4)
\]

Or (approx):

\[
I_{ds,\text{subth}}^{\text{approx}} = I_0 \frac{W}{W_0} 10^{\frac{V_{GS}-V_{TH}}{S}}
\]

\[
S = 2.3m \frac{kT}{q}
\]

Leakage Components

![Leakage Components Diagram](image)
Leakage Components (250nm)

1. pn junction reverse bias current
2. Weak inversion
3. Drain-induced barrier lowering (DIBL)
4. Gate-induced drain leakage (GIDL)
5. Punchthrough
6. Narrow width effect
7. Gate oxide tunneling
8. Hot carrier injection

Leakage Components

- Drain-induced barrier lowering (DIBL)
  - Voltage at the drain lowers the source potential barrier
  - Lowers \( V_{\text{thr}} \), no change on \( S \)
- Gate-induced drain leakage (GIDL)
  - High field between gate and drain increases injection of carriers into substrate -> leakage
  - (band-to-band leakage)
2.H Transistor C-V

MOS Transistor as a Switch

Discharging a capacitor

- Can solve:
  \[ i_{DS} = i_{DS}(v_{DS}) \]
  \[ i_{DS} = C(v_{DS}) \frac{dv_{DS}}{dt} \]

- Prefer using equivalent resistances
- Find \( t_{pHL} \)
- Find equivalent \( C, R \)

\[ t_{pHL} = \int \frac{C(v_{DS})dv_{DS}}{i_{DS}(v_{GS}, v_{DS})} \]
MOS Capacitances

• Gate capacitance
  • Non-linear channel capacitance
  • Linear overlap, fringing capacitances
    • Miller effect on overlap, fringing capacitance
  • Non-linear drain diffusion capacitance
    • PN junction

• Wiring capacitances
  • Linear

Gate and Drain Capacitances

Gate capacitance

Drain capacitance
Gate Capacitances

• Gate capacitance is non-linear
  • First order approximation with $C_{ox}WL$ ($C_{ox}L = 2fF/\mu m$)
  • Need to find the actual equivalent capacitance by simulating it
  • Since this is a linear approximation of non-linear function, it is valid only over the certain range
    • Different capacitances for HL, LH transitions and power computation
• Drain capacitance non-linearity compensates
  • But this changes with fanout
2.1 Delay Revisited

MOS Transistor as a Switch (EECS251A)

\[
R_{eq} = \text{average}_{t_1, t_2} (R_{on}(t)) = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} R_{on}(t) dt = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} V_{GS}(t) I_D(t) dt
\]

\[
\approx \frac{1}{2} (R_{on}(t_1) + R_{on}(t_2))
\]
**MOS Transistor as a Switch (EE241A)**

Solving the integral:

\[
R_{eq} = \frac{1}{-V_{DD}/2} \int_{-V_{DD}/2}^{V_{DD}/2} \frac{V}{I_{DSAT}(1 + \lambda V_{DS})} dV = \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{7}{9} \lambda V_{DD}\right)
\]

with appropriately calculated \( I_{dsat} \)

**Averaging resistances:**

\[
R_{eq} = \frac{1}{2} \left( \frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)} \right) = \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{5}{6} \lambda V_{DD}\right)
\]

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**CMOS Performance**

**Propagation delay:**

\[
t_{pHL} = (\ln 2)R_{eqn}C_L \quad t_{pLH} = (\ln 2)R_{eqp}C_L
\]

\[
\ln 2 = 0.7
\]
Effective Current

- $I_{on}(V_{DD})$ is never reached
- Define $I_{eff} = (I_H + I_L)/2$
- $I_L = I_{DS}(V_{GS} = V_{DD}/2, V_{DS} = V_{DD}); I_H = I_{DS}(V_{GS} = V_{DD}, V_{DS} = V_{DD}/2)$,
DIBL Matters

- A. Loke, VLSI’16

FinFET, FDSOI – less DIBL

\[ I_{\text{eff}} = \frac{I_L + I_H}{2} \]

\[ I_L @ V_{GS} = \frac{1}{2} V_{DD}, \ V_{DS} = V_{DD} \]

\[ I_H @ V_{GS} = V_{DD}, \ V_{DS} = \frac{1}{2} V_{DD} \]

\[ I_{\text{eff}} \text{ is better than } I_{\text{DSat}} \]

for estimating inverter \( CV/I \) switching delay

Less DIBL \( \rightarrow \) higher \( I_{\text{eff}} \) \& \( r_{out} \) for same \( I_{\text{DSat}} \)

Transistor Stacks

\[ I_{ds}[A] \]

\[ V_{ds}[V] \]
Effective Current in Stacks

- Add linear current, $I_3$

Von Arnim, IEDM’2007

Next Lecture

- Standard cells, design kit