Qualcomm to acquire NUVIA for 1.4B
Announcements

• Lab 1 posted, due on Thursday

• Assignment 1 + Lab 2 will be posted this week
Assigned Reading

Outline

• Features of modern technologies
  • Process technologies
• Transistor models
3. Strained Silicon

Compressive channel strain
30% drive current increase
in 90nm CMOS

Tensile channel strain
10% drive current increase
in 90nm CMOS

Intel
Intel’s Strained Si Numbers

Performance gains:

<table>
<thead>
<tr>
<th></th>
<th>90 nm</th>
<th></th>
<th>65 nm</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>NMOS</td>
<td>PMOS</td>
<td>NMOS</td>
</tr>
<tr>
<td>μ</td>
<td>20%</td>
<td>55%</td>
<td>35%</td>
</tr>
<tr>
<td>IDSAT</td>
<td>10%</td>
<td>30%</td>
<td>18%</td>
</tr>
<tr>
<td>IDLIN</td>
<td>10%</td>
<td>55%</td>
<td>18%</td>
</tr>
</tbody>
</table>

S. Thompson, VLSI’06 Tutorial
Sizing PMOS/NMOS

- No strain
  \[ W_1 = 1 \quad W_2 \sim 2 \]

- Strained Si
  \[ W_1 = 1 \quad W_2 = 1.6 \]
5. Thin-Body Devices

• 28nm FDSOI

• 22/14nm finFET

N. Planes, VLSI’2012

C. Auth, VLSI’2012
Sizing PMOS/NMOS

• \( \sim 28\text{nm} \)

• FinFET

\[ W_1 = 1 \quad \text{and} \quad W_2 = 1.6 \]

Diagram with input (In), output (Out), and power supply (V_{DD}).
5. FinFETs

- FinFET scaling

<table>
<thead>
<tr>
<th>22/20nm</th>
<th>16/14nm</th>
<th>10nm</th>
</tr>
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<tbody>
<tr>
<td>Intel, IEDM’12</td>
<td>Intel, VLSI’14</td>
<td>Intel, IEDM’17</td>
</tr>
</tbody>
</table>

- N-P spacing

Garcia Bardon, IEDM’16

- Track scaling
5. FDSOI

- 2012: 28FD-SOI (STMicroelectronics)
- 2013: 28FD-SOI (Samsung)
- 2014: 22FDX (GLOBALFOUNDRIES)
- 2015: 12FDX (GLOBALFOUNDRIES)
- 2016: 18FDS (Samsung)
5. Interconnect
Interconnect: CMP

Cu interconnect: Dual damascene process

- Ta barrier layer to prevent Cu from diffusing into Si
- Etch stop (SiN)

- Metal density rules (20%-80%)
- Slotting rules
- Also: Antenna rules
Module 2: Transistor and Gate Models
Module 2 Goals

• Models that traverse design hierarchy
• Start with transistor models
• Gate delay models
• Use models to time the design
• Modeling variability

• Based on 251A, approach
  • Start simple
  • Increase accuracy, when needed
2. A MOS Modeling Goals
Device Models

• Transistor models
  • I-V characteristics
  • C-V characteristics

• Interconnect models
  • R, C, L
  • Covered in EE240A
Transistor Modeling

• Different levels:
  • Hand analysis
  • Computer-aided analysis (e.g. Matlab)
  • Switch-level simulation (some flavors of ‘fast Spice’)
  • Circuit simulation (Hspice)

• These levels have different requirements in complexity, accuracy and speed of computation

• We are primarily interested in delay and energy modeling, rather than current modeling

• But we have to start from the currents…
Transistor Modeling

• DC
  • Accurate I-V equations
  • Well behaved conductance for convergence (not necessarily accurate)

• Transient
  • Accurate I-V and Q-V equations
  • Accurate first derivatives for convergence
  • Conductance, as in DC

• Physical vs. empirical

from BSIM group
Goal for Today

• Develop velocity-saturated model for $I_{on}$ and apply it to sizing and delay calculation
  • Similar approach as in 251A, just use an analytical model
Transistor I-V Modeling

• BSIM
  • Superthreshold and subthreshold models
  • Need smoothening between two regions

• EKV/PSP
  • One continuous model based on channel surface potential
2.B Long-Channel MOS On-Current
MOS I-V (BSIM)

Start with the basics:

\[ I_{DS} = W C_{ox} (V_{GS} - V_{Th} - V_C(x)) \mu E \]
MOS I-V (BSIM)

Start with the basics:

\[ I_{DS} = WC_{ox}(V_{GS} - V_{Th} - V_{C}(x)) \mu E \]

\[ I_{DS} = WC_{ox}(V_{GS} - V_{Th} - V_{C}(x)) \mu (dV_{C}(x)/dx) \]

• When integrated over the channel:

\[ I_{DS} = \frac{W}{L} \mu C_{ox} \left( V_{GS} - V_{Th} - \frac{V_{DS}}{2} \right) V_{DS} \]

Transistor saturates when \( V_{GD} = V_{Th} \) - the channel pinches off at drain's side.

\[ I_{DS} = \frac{W}{2L} \mu C_{ox} \left( V_{GS} - V_{Th} \right)^2 \]
MOS Currents (32nm CMOS with $L >> 1 \mu m$)

Currents according to the quadratic model
Correct for long channel devices ($L \sim \mu m$)
Simulated 32nm Transistor

$L = 32\text{nm}$

$V_{DS} [\text{V}]$

$I_{DS} [\text{A}]$

~ Linear
Simulation vs. Model

Major discrepancies:
• shape
• saturation points
• output resistances
2.C Velocity Saturation
Velocity Saturation

\[ E_c = \frac{v_{sat}}{\mu_{eff}} \]

\( v_{sat} = 10^5 \text{ m/s} \)

Constant velocity

Constant mobility (slope = \( \mu \))

\( E_c = 1.5 \)

\( E(V/\mu m) \)

\( v_n (\text{m/s}) \)
Modeling Velocity Saturation

- Fit the velocity-dependence curve

\[ V = \frac{\mu_{\text{eff}} E}{\left(1 + \left(\frac{E}{E_C}\right)^n\right)^{1/n}} \]

NMOS: \( n = 2 \)
PMOS: \( n = 1 \)
Modeling Velocity Saturation

• A few approximations: (a) $n \to \infty$, (b) $n = 1$, (c) piecewise

\[ E_c/2 = \frac{v_n}{\mu} \]
2.D Short-Channel MOS On-Current
Approximation $n \to \infty$

1) $v = \mu_{\text{eff}}E, \ E < E_c$

$$I_{DS} = \mu_{\text{eff}} C_{ox} \frac{W}{L} \left( (V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2} \right)$$

2) $v = v_{sat}, \ E > E_c$

$$I_{Dsat} = \mu C_{ox} \frac{W}{L} \left( (V_{GS} - V_{Th})V_{Dsat} - \frac{V_{Dsat}^2}{2} \right)$$

$V_{Dsat} = ?$

Can be reduced to Rabaey DIC model by $V_{Dsat} = \text{const}$
\[ I_D = 0 \text{ for } V_{GT} \leq 0 \]

\[ I_D = k' \frac{W}{L} \left( V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) \left( 1 + \lambda V_{DS} \right) \text{ for } V_{GT} \geq 0 \]

with \( V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT}) \),

\[ V_{GT} = V_{GS} - V_T, \]

and \( V_T = V_{T0} + \gamma \left( \sqrt{1 - 2 \phi_F + V_{SB}} - \sqrt{1 - 2 \phi_F} \right) \)

\( \gamma \) - body effect parameter

From Rabaey, 2nd ed.
Unified MOS Model

• Model presented is compact and suitable for hand analysis.

• Still have to keep in mind the main approximation: that $V_{DSat}$ is constant. When is it going to cause largest errors?
  • When does $E$ scale? – Transistor stacks.

• But the model still works fairly well.
  • Except for stacks
Approximation $n = 1$, piecewise

- $n = 1$ is solvable, piecewise closely approximates

$$v = \begin{cases} \frac{\mu_{\text{eff}} E}{1 + E/E_0}, & E < E_0 = \frac{2v_{\text{sat}}}{\mu_{\text{eff}}} \\ v_{\text{sat}}, & E > E_0 \end{cases}$$

Sodini, Ko, Moll, TED’84
Toh, Ko, Meyer, JSSC’88
BSIM model
Drain Current

• We can find the drain current by integrating

\[ I_{DS} = W C_{ox} (V_{GS} - V_{Th} - V_C(x)) \]

\[
I_{DS} = \frac{\mu C_{ox}}{1 + (V_{DS}/E_CL)} \frac{W}{L} \left( (V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2} \right)
\]

› In saturation:

\[ I_{DSat} = C_{ox} W V_{sat} (V_{GS} - V_{Th} - V_{Dsat}) \]

\[
I_{Dsat} = \frac{\mu C_{ox}}{1 + (V_{Dsat}/E_CL)} \frac{W}{L} \left( (V_{GS} - V_{Th})V_{Dsat} - \frac{V_{Dsat}^2}{2} \right)
\]
Drain Current in Velocity Saturation

- Solving for $V_{DSat}$

$$V_{DSat} = \frac{(V_{GS} - V_{Th})E_C L}{(V_{GS} - V_{Th}) + E_C L}$$

- And saturation current

$$I_{DSat} = \frac{W \mu_{eff} C_{ox} E_C L}{L} \frac{(V_{GS} - V_{Th})^2}{2} \frac{(V_{GS} - V_{Th})}{(V_{GS} - V_{Th}) + E_C L}$$
Velocity Saturation

$V_{DS}[V]$ vs $I_{DS}[A]$ graph showing the relationship between drain-source voltage and drain-source current for different values of $V_{DS}$. The graph illustrates the saturation region of the transistor, with the current increasing as the voltage increases, up to a point where the current plateaus, indicating saturation.
Velocity Saturation

- $E_C L$ is $V_{GS}$ dependent
- Can calculate $V_{DSat}$ ($V_{Th} \sim 0.4V$ in 28nm)

<table>
<thead>
<tr>
<th>$V_{GS} [V]$</th>
<th>0.5</th>
<th>0.6</th>
<th>0.7</th>
<th>0.8</th>
<th>0.9</th>
<th>1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DSat} [V]$</td>
<td>0</td>
<td>0.05</td>
<td>0.11</td>
<td>0.18</td>
<td>0.25</td>
<td>0.33</td>
</tr>
</tbody>
</table>

- For $V_{GS} - V_{Th} \ll E_C L$, $V_{DSat}$ is close to $V_{GS} - V_{Th}$
- For large $V_{GS}$, $V_{DSat}$ bends upwards toward $E_C L$
- Therefore $E_C L$ can be sometimes approximated with a constant term
Next Lecture

• Transistor models