Announcements

• Assignment 2 due this week
  • Followed by a quiz next Tuesday

• Create webpages (github) for your projects!
  • And e-mail me the links!

• Midterm reports due next week
Midterm Reports

Outline

• Flip-flop design
3. Design for Performance

3.F Flip-Flops

Key Point

• Two ways to design a flip-flop
  • Latch pair (large majority)
  • Pulsed latch
Latch vs. Flip-Flop

Flip-Flops

- Performance metrics
- Delay metrics
  - Insertion delay
  - Inherent race immunity
  - ‘Softness’ (Clock skew absorption)
  - Inclusion of logic
  - Small (+constant) clock load
- Power/Energy Metrics
  - Power/energy
- Design robustness
  - Noise immunity
Types of Flip-Flops

Latch Pair

Pulse-Triggered Latch
Latch Pair as a Flip-Flop

Sources of Noise

1. Noise on input
2. Leakage
3. α-Particle and cosmic rays
4. Unrelated signal coupling
5. Power supply ripple
Latch Pairs

- Example: PowerPC 603 (Gerosa, JSSC 12/94)

Flip-Flop Clk-Q, setup, hold
Flip-Flop Timing Characterization

- Combinational logic delay is a function of output load and input slope

- Sequential timing (flip-flop):
  - $t_{clk-q}$ is function of output load and clock rise time
  - $t_{Su}$, $t_H$ are functions of D and Clk rise/fall times

Pulse-Triggered Latches

- First stage is a pulse generator
  - generates a pulse (glitch) on a rising edge of the clock

- Second stage is a latch
  - captures the pulse generated in the first stage

- Pulse generation results in a negative setup time

- Frequently exhibit a soft edge property

- Note: power is always consumed in the pulse generator
  - Often shared by a group (register)
Pulsed Latch

Simple pulsed latch

(a) Sub-nano Pulse Generator

(b) Pulse Register

Kozu, ISSCC’96

Intel/HP Itanium 2

Intel/HP Itanium 2
Pulsed Latches

Hybrid Latch Flip-Flop, AMD K-6
Partovi, ISSCC’96

HLFF Operation

1-0 and 0-1 transitions at the input with 0ps setup time
Hybrid Latch Flip-Flop

Skew absorption

Pulsed Latches

AMD K-7

Inputs are dynamically received
Clock edge is hard

To 3 other flip-flops

**Pulsed Latches**

Used in an automated P&R flow

Partovi, VLSI'12

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**Pulsed Latches**

7474, from mid-1960's
Pulsed Latches

First stage is a sense amplifier, precharged to high, when $Clk = 0$
After rising edge of the clock sense amplifier generates the pulse on $S$ or $R$
The pulse is captured in S-R latch
Cross-coupled NAND has different propagation delays of rising and falling edges

DEC Alpha 21264, StrongARM 110

Sense Amplifier-Based Flip-Flop

Sampling Window Comparison

Next Lecture

- Memory