Announcements

- Quiz today
- New labs posted
- New assignment this week
- Response to project proposals this week
  - Project web pages

Samsung’s 3nm GAA SRAM (ISSCC’21)
Outline

• Variability
• Timing with variations
**Layout: Poly Proximity Effects**

- Gate CD is a function of its neighborhood

[Diagram showing proximity effects in layout]

Gate length depends on:
- Light intensity profile falling on the resist
- Resist: application of developer fluid\(^1\), post exposure bake (PEB) temperature\(^2\)
- Dry etching: microscopic loading effects\(^3\)

\(^1\) J. Cain, M.S. Thesis, UC Berkeley
\(^2\) D. Steele et al., SPIE, vol.4689, July 2002.

**Layout: Proximity Test Structures**

- 90nm experiments
- 45nm experiments

[Diagram showing test structures for 90nm and 45nm experiments]

L.T. Pang, VLSI’06

Ring oscillators and individual transistor leakage currents

L.T. Pang, CICC’08

No single gates allowed

P1 min max2 P2 mid1

P3 max1 P4 max2
Results: Single Gates in 90nm

- Max $\Delta F$ between layouts $> 10\%$
- Within-die $3\sigma/\mu \sim 3.5\%$, weak dependency on density

Results: Single Gates in 45nm

- Weak effect on performance. $\Delta F \sim 2\%$
- Small shifts in NMOS leakage and bigger shifts in PMOS leakage
Impact of Stress

- 45nm STM process: Wafer rotated <100> - higher PMOS mobility
- NMOS strained through capping layer
- Subatmospheric STI – weak tensile stress

45nm STM process: Wafer rotated <100> - higher PMOS mobility
NMOS strained through capping layer
Subatmospheric STI – weak tensile stress

Impact of Longer Diffusion in 45nm

- Strongest effect measured in 45nm, ΔF ~ 5%
- No significant shift in $I_{LEAK}$

22 chips from 2 wafers
Impact of Shallow Trench Isolation (STI)

- $\Delta F \sim 3\%$, small changes in $I_{\text{LEAK}}$
- Due to STI-induced stress

Impact of Correlations
Chip Yield Depends on Inter-Gate Correlation

- Yield = Pr (sum of n delays < clock period)
- \( \rho = 0 \) gives highest yield through averaging

Non-correlated gates in a path reduce impact of variation

Bowman et al, JSSC, Feb 2002

Chip Yield Depends on Inter-Path Correlation

- Yield = Pr (max delay of K paths < clock period)
- K = 1 gives highest yield

Correlated paths reduce impact of variation

Bowman et al, JSSC, Feb 2002
Process Corners

2. P Design Variability
Some Random Effects
Random Dopant Fluctuations

- Number of dopants is finite

Frank, IBM J R&D 2002

$\sigma_{VT} = 23\text{mV}$

$\sigma_{VT} = 52\text{mV}$
Processing: Line-Edge Roughness

• Sources of line-edge roughness:
  • Fluctuations in the total dose due to quantization
  • Resist composition
  • Absorption positions

Effect:
  • Variation (random) in leakage and power

Oxide Thickness

• Systematic variations
• Roughness in the Si/SiO2 interface
  • Smaller effect than RDF

Asenov, TED’2002
### Transistor Matching

- $V_{Th}$ matching of geometrically identical transistors varies with size
- \( \sim \sqrt{WL} \) and distance

- Pelgrom parameter $A_{VT}$
  - Scales with technology (EOT)

- $A_{VT}$ in FDSOI technology

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### Negative Bias Temperature Instability

- PFET $V_{Th}$'s shift in time, at high negative bias and elevated temperatures
- The mechanism is thought to be the breaking of hydrogen-silicon bonds at the Si/SiO2 interface, creating surface traps and injecting positive hydrogen-related species into the oxide.
- Also other charge trapping and hot-carrier defect generation
- Systematic + random shifts
Random Telegraph Signal (RTS)

- Trapping of a carrier in oxide traps modulates $V_{th}$ or $I_{ds}$
- $\tau_e$ and $\tau_c$ are random and follow exponential distributions

$\Delta V_{th, RTS} \sim \frac{1}{WL}$
$\Delta V_{th, RDF} \sim \frac{1}{\sqrt{WL}}$

RTS and Technology Scaling

- RTS exceeds RDF at 3 sigma with 20nm gates

Tega et al, IRPS 2008.

Tega et al, VLSI Tech. 09
3. Design for Performance

3.A Flip-Flop Timing

Example Clock System

Clock Nonidealities

- Clock skew
  - Spatial variation in temporally equivalent clock edges; deterministic + random, $t_{SK}$

- Clock jitter
  - Temporal variations in consecutive edges of the clock signal; modulation + random noise
  - Cycle-to-cycle (short-term) - $t_{JS}$
  - Long-term - $t_{JL}$

- Variation of the pulse width
  - for level-sensitive clocking
Clock Uncertainties

Sources of clock uncertainty

Flip-Flop Parameters

Delays can be different for rising and falling data transitions
Latch Parameters

Delays can be different for rising and falling data transitions

Clock Constraints in Edge-Triggered Systems

\[ t_{CL} \leq (t_{CY} - t_{SK} - t_{JS}^\text{S}) - (t_{SU}^\text{H} + t_{CQ}) \]
\[ t_{CL} \geq t_{SK} + (t_{H} - t_{CQ}) \]
3. B Timing with Uncertainty/Variations

Pictorial View of Setup and Hold Tests
Handling of Across-Chip Variation

- Each gate has a range of delay: \([lb, ub]\)
  - The lower bound is used for early timing
  - The upper bound is used for late timing
- This is called an early/late split
- Static timing obtains bounds on timing slacks
  - Timing is performed as one forward pass and one backward pass

<table>
<thead>
<tr>
<th>Setup test</th>
<th>Hold test</th>
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<tbody>
<tr>
<td><img src="image1.png" alt="Diagram" /></td>
<td><img src="image2.png" alt="Diagram" /></td>
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How is the Early/Late Split Computed?

- The best way is to take known effects into account during characterization of library cells
  - History effect, simultaneous switching, pre-charging of internal nodes, etc.
  - This drives separate characterization for early and late; this is the most accurate method
- Failing that, the most common method is derating factors
  - Example: Late delay = library delay \* 1.05  
    Early delay = library delay \* 0.95
- The IBM way of achieving derating is LCD factors (Linear Combination of Delay) (FC=fast chip, SC=slow chip, see next page)
  - Late delay = \(\alpha_L \cdot FC\_delay + \beta_L \cdot NOM\_delay + \gamma_L \cdot SC\_delay\)
  - Early delay = \(\alpha_E \cdot FC\_delay + \beta_E \cdot NOM\_delay + \gamma_E \cdot SC\_delay\)
- Across-chip variation is therefore assumed to be a fixed proportion of chip-to-chip variation for each cell type
IBM Delay Modeling*

At a given corner
late delay = intrinsic + systematic + random
early delay = intrinsic – systematic – random

*P. S. Zuchowski, ICCAD’04

Traditional Timing Corners

Intra-chip variation
Chip-to-chip variation
The Problem with an Early/Late Split

- The early/late split is very useful
  - Allows bounds during delay modeling
  - Any unknown or hard-to-model effect can be swept under the rug of an early/late split
- But, it has problems
  - Additional pessimism (which may be desirable)
  - Unnecessary pessimism (which is never desirable)

How to Have Less Pessimism?

- Common path pessimism removal
- Account for correlations
- Credit for statistical averaging of random
Statistical Timing

• Deterministic

\[ A = a_0 + \sum_{i=1}^{n} a_i \Delta X_i + a_{n+1} \Delta R_a \]

\[ B = b_0 + \sum_{i=1}^{n} b_i \Delta X_i + b_{n+1} \Delta R_b \]

\[ \sigma_A = \sqrt{\sum_{i=1}^{n+1} a_i^2} \]

\[ \sigma_B = \sqrt{\sum_{i=1}^{n+1} b_i^2} \]

\[ \rho = \frac{\sum_{i=1}^{n+1} a_i b_i}{\sigma_A \sigma_B} \]

\[ \theta \equiv (\sigma_A^2 + \sigma_B^2 - 2\rho \sigma_A \sigma_B)^{1/2} \]

\[ t = \phi \left[ \left( \frac{a_0 - b_0}{\theta} \right) \right] \]

\[ E[\max(A, B)] = a_0 t + b_0 (1 - t) + \theta \phi \left[ \left( \frac{a_0 - b_0}{\theta} \right) \right] \]

\[ E[\max(A, B)]^2 = (\sigma_A^2 + \sigma_B^2) t + (\sigma_A^2 + \sigma_B^2)(1 - t) + (a_0 + b_0) \theta \phi \left[ \left( \frac{a_0 - b_0}{\theta} \right) \right] \]


** M. Cain, “The moment-generating function of the minimum of bivariate normal random variables,” American Statistician, May ’94, 48(2)
Unified View of Correlations

\[ D = a_0 + \sum a_i \Delta X_i + a_r \Delta X_r \]

- Independently random part
- Spatially correlated part: within-chip distance-related correlation
- Globally correlated part: chip-to-chip, wafer-to-wafer, batch-to-batch variation

Spatial Correlation vs. Early/Late Split

Dependence on common virtual variables cancels out at the timing test
Next Lecture

• Latch timing
• Flip-flops