Design and Analysis of Distributed Amplifiers

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Abstract-- This report will highlight the design of practical distributed amplifiers. The design approach includes the various loss mechanisms inherent in the FET transistor as well as transmission line losses and passive device losses. The design goal is to achieve a flat gain over a large bandwidth while achieving the lowest noise possible. A practical design is also illustrated.

Index Terms-- Distributed Amplifiers, Traveling Wave Amplifiers

I. Introduction

A schematic of a distributed amplifier [1][2] is shown in Fig. 1. The distributed amplifier is composed of two coupled lumped transmission lines. Power is coupled from the "gate-line" to the "drain-line" through transistors M_1-M_n whereas power is coupled in the reverse direction parasitically through the feedback capacitor C_{gd} of the transistors. Since for a practical transistor $S_{21} >> S_{12}$, the behavior of the amplifier is dominated by the "forward-direction" coupling of power from the gate line to the drain line. As evident from the figure, the parasitics of the transistor form an integral part of the amplifier completing the transmission lines. In this way, the parasitics of the amplifier do not limit the gain-bandwidth product of the amplifier as in a traditional amplifier, allowing large bandwidths to be achieved. If care is exercised in equalizing the phase velocity on the gate and drain line, then power interferes constructively and the overall gain of the amplifier is enhanced by the addition of each stage.

The number of stages that may be used is limited by the inherent losses on the drain and gate line. Thus, the additional attenuation incurred by the addition of a stage may outweigh the benefits of gain and thus there is an optimum number of stages for gain. This will always occur since the gain is a polynomial of the number of stages whereas the transmission line attenuation is a decaying exponential function of the length of the transmission line.

In section II we will review the image parameter method as it relates to designing a distributed amplifier. Specially, the inherent losses of the transistor and microstrips will be taken into account to find the line impedance, propagation and attenuation constants. These results will be used in section III where we derive the gain of a distributed amplifier. In section IV we review the design procedure of Beyer et al. [3]. In section V we discuss the noise figure of a distributed amplifier and finally in section VI we will discuss the design of a distributed amplifier using the FET-217 transistor [4]. The design achieves more than 10 GHz of bandwidth with 1dB of gain flatness with 17 dB power gain.

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II. Image Parameter Method

The image parameter method may be applied to the distributed amplifier since it consists of a cascade of identical two-port networks forming an artificial transmission line. The image impedance Z_i for a reciprocal symmetric two-port is defined as the impedance looking into port 1 or 2 of the two-port when the other terminal is also terminated in Z_i. This impedance is given by [5]

$$Z_i = \sqrt{\frac{B}{C}} \tag{1}$$

where the ABCD matrix of the two-port is given by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} \tag{2}$$

where $A = D$ by symmetry. The propagation constant for the current and voltage is given by

$$e^{-g} = \sqrt{AD} - \sqrt{BC} \tag{3}$$

Thus, wave propagation occurs if γ has an imaginary component. For the *T*-network shown in Fig. 2, the image impedance and propagation factors are given by

$$Z_i = \sqrt{Z_1 Z_2}\sqrt{1+\frac{Z_1}{4Z_2}} \tag{4}$$

$$e^{g} = 1+\frac{Z_1}{2Z_2}+\sqrt{\frac{Z_1}{Z_2}+\frac{Z_1^2}{4Z_2^2}} \tag{5}$$

A. Lossless Lumped Transmission Line

For a lossless cascade of *T*-sections such as shown in Fig. 3, the propagation factor and image impedance are given by [5]

$$Z_i = \sqrt{\frac{L}{C}\left(1-\left(\frac{w}{w_c}\right)^2\right)} \tag{6}$$

$$e^{g} = 1-\frac{2w^2}{w_c^2}+\frac{2w}{w_c}\sqrt{\frac{w^2}{w_c^2}-1} \tag{7}$$

$$w_c = \frac{2}{\sqrt{LC}} \tag{8}$$

Thus, for $w < w_c$ the lossless structure has a real image impedance and a purely imaginary propagation factor. Beyond the cutoff frequency, w_c the propagation factor has a real component that increases without bound. These results are consistent with the distributed transmission line since $w_c \to \infty$ for such a structure.

B. Lossy Lumped Transmission Line

Figures 4 and 5 show the lossy "gate" and "drain" transmission line. The losses are due to the lossy microstrips or spiral inductors as well as the losses of the input/output impedance looking into the gate/drain of the FET. A series gate resistance models the FET losses. The inductor losses are divided into two components, one part r_x modeling the metalization losses in series with the inductor and one component R_x modeling the substrate losses. For an insulating substrate, the conductive substrate losses are negligibly small and so R_x=0. If dielectric losses are present, it is more appropriate to place R_x in shunt rather than in series with the substrate capacitance.

In reality these loss resistors are frequency dependent owing to skin and proximity effects and displacement current in the substrate [6] but for simplicity we will assume a constant value. If the substrate is sufficiently conductive and near the microstrip metal layers, induced eddy currents lead to an additional loss mechanism. This is the case for highly conductive substrates used in epi CMOS processes. Again, we neglect this loss in the following analysis.

Using the notation of the previous section, the *T*-section impedance and admittance are

$$Z_{1g} = jwL_g + r_{xg} \tag{9}$$

$$Y_{2g} = \frac{jwC_{gs}(1+2\frac{C_{xg}}{C_{gs}}) - w^2 C_{gs}(\frac{1}{w_{xg}} + \frac{C_{xg}}{w_g C_{gs}})}{(1+j\frac{w}{w_g})(1+j\frac{w}{w_{xg}})} \tag{10}$$

where

$$w_g = \frac{1}{C_{gs}R_i} \qquad w_{xg} = \frac{1}{C_{xg}R_{xg}}$$

Similarly, for the lossy drain line, the *T*-section impedance and admittance are

$$Z_{1d} = jwL_d + r_{xd} \tag{11}$$

$$Y_{2d} = \frac{G_{ds}(1-\frac{w^2}{w_{xd}w_{ds}}) + jw(\frac{2G_{xd}}{w_{xd}} + \frac{G_{ds}}{w_{ds}} + \frac{G_{ds}}{w_{xd}})}{(1+j\frac{w}{w_{xd}})} \tag{12}$$

where

$$w_d = \frac{1}{C_{ds}R_{ds}} \qquad w_{xd} = \frac{1}{C_{xd}R_{xd}}$$

Using (9)-(12), the image impedance and propagation factor can be calculated using (4) and (5). These expressions are plotted in figures 6, 7, and 8. The plots are generated using the following gate and drain parameters[1]

$$\begin{aligned} L_g &= 1.85nH & r_{xg} &= w_{Lg}L_g \\ C_{gs} &= 310\,fF & R_i &= 7.25\Omega \\ C_{xg} &= 50\,fF & R_{xg} &= \frac{1}{w_{xg}C_{xg}} \\ L_d &= 2.04nH & r_{xd} &= w_{Ld}L_d \\ C_{ds} &= 96\,fF & R_{ds} &= 385\Omega \\ C_{xd} &= 50\,fF & R_{xd} &= \frac{1}{w_{xd}C_{xg}} \end{aligned} \tag{13}$$

The FET parameters come from the standard FET-217 transistor model whereas the drain and gate inductor parasitics are shown parameterized as a function of the cutoff frequencies. In Fig. 6 we also include the lossless image impedance given by (6) for comparison.

As evident from the figures, even for lossless passive devices the losses in the intrinsic FET warrant careful analysis. Additionally, the frequency dependence of the image impedance can potentially destroy the broadband operation of the device if it is not matched correctly.

C. Image Impedance Matching

To achieve an impedance match over a broad range, the load and source impedance must be transformed into the line image impedance. Otherwise, the gain response will not be flat as a function of frequency.

The bisected-π *m*-derived section shown in Fig. 9, serves this purpose well [5]. In Fig. 10 we plot the impedance looking into the gate and drain line when transformed by the *m*-derived section. As evident from the figures, the impedance is approximately constant over a broad range of frequencies, a big improvement over the frequency variation of the image impedance in Fig. 6. The *m*-derived impedance matching network can also be used to match directly to 50 Ω.

The performance of the *m*-derived section shown in Fig. 10 is shown for the lossy transmission line as well as the ideal transmission line. Its performance is not as good in the lossy case but it can be flattened with further optimization.

III. Distributed Amplifier Gain

Given the background of Section II, we are now in a good position to derive the gain of the distributed amplifier. The following derivation closely follows the work of [3] but deviates in that we work directly with the complete expressions for the transmission line parameters as opposed to the approximate expressions developed by [3].

[1] These values correspond to the design presented in section VI.

A. Expression for Gain

Using the simplified FET model shown in Fig. 11, the total output current of an *n*-stage distributed amplifier shown in Fig. 1 can be written as

$$I_o = \tfrac{1}{2} g_m e^{-g_d/2} \sum_{k=1}^{n} V_{ck} e^{-(n-k)g_d} \tag{14}$$

where g_d is the propagation delay of the drain line given by (5) and V_{ck} is the voltage drop across the *k*th stage input capacitor. Note that we have assumed constructive interference of the FET currents since in a practical design the phase velocity of the drain line is matched to the gate line by adding additional shunt drain capacitance to satisfy

$$b = \mathrm{Im}\{g_g\} = \mathrm{Im}\{g_d(C_p)\} \tag{15}$$

In the low loss case this is equivalent to

$$\frac{2}{\sqrt{L_g(C_{gs}+2C_{xg})}} = \frac{2}{\sqrt{L_d(C_{ds}+2C_{xd}+C_p)}} \tag{16}$$

The above relation can be used as a starting point solution in a non-linear iteration loop to solve (15). Eq. (15) represents a continuum of equations since it varies as a function of *w*, and therefore it can be satisfied in the least squared sense over the range of interest by minimizing

$$\int_0^{w_c} \left(\mathrm{Im}(g_g) - \mathrm{Im}(g_d)\right)^2 dw \tag{17}$$

The voltage across the *k*th stage input capacitor is given by

$$V_{ck} = \frac{V_i d \exp\left(\frac{-(2k-1)g_g}{2} - j\tan\frac{w}{w_g}\right)}{\sqrt{1+\left(\frac{w}{w_g}\right)^2}} \tag{18}$$

The origin of the exponential term is due to the finite propagation velocity along the gate line as well as the frequency dependent voltage division between the input capacitance and the resistance. The term δ is the voltage at the center of the *T*-section. This can be derived with the aid of Fig. 12. Note that

$$\begin{aligned} I_1 e^{g} &= Y_2 V_C + I_1 \\ \frac{V_c - V_1}{Z_1/2} &= I_1 \end{aligned} \tag{19}$$

Using the above relations to eliminate I_1 one obtains

$$\frac{V_C}{V_1} = \frac{e^g - 1}{e^g - \left(1 + \frac{Z_1}{2Z_2}\right)} \tag{20}$$

Making use of (5) one obtains

$$d \equiv \frac{V_C}{V_1} = \frac{\frac{Z_1}{2Z_2} + \sqrt{\frac{Z_1}{Z_2} + \left(\frac{Z_1}{2Z_2}\right)^2}}{\sqrt{\frac{Z_1}{Z_2} + \left(\frac{Z_1}{2Z_2}\right)^2}} \tag{21}$$

Using (18) in (14) one obtains

$$I_o = \frac{g_m V_i d \sinh\left[\frac{n}{2}(a_d - a_g)\right] e^{\frac{-n(a_d+a_g)}{2}} e^{-jnf - j\tan^{-1}\frac{w}{w_g}}}{2\sqrt{1+\left(\frac{w}{w_g}\right)^2}\sinh\left[\frac{1}{2}(a_d - a_g)\right]} \tag{22}$$

To find the power gain, we use the following expressions

$$P_o = \tfrac{1}{2}|I_o|^2 \,\mathrm{Re}\left[Z'_{id}\right] \tag{23}$$

$$P_i = \frac{|V_i|^2}{2|Z_{ig}|^2}\mathrm{Re}\left[Z'_{ig}\right] \tag{24}$$

to obtain

$$G = \frac{\mathrm{Re}\left[Z'_{id}\right]}{\mathrm{Re}\left[Z'_{ig}\right]}\left|Z'_{ig}\right|^2 \frac{g_m^2 |d|^2 \sinh^2\left[\frac{n}{2}(a_d - a_g)\right] e^{-n(a_d+a_g)}}{4\left[1+\left(\frac{w}{w_g}\right)^2\right]\sinh^2\left[\frac{1}{2}(a_d - a_g)\right]} \tag{25}$$

where the primed impedances are the transformed line image impedance (using, for instance, an *m*-derived matching section).

B. Design Tradeoffs

The above expression is the gain as a function of the drain/gate transmission line parameters, assuming fixed FET parameters. In reality, the FET width and length may be scaled as well. But typically for highest frequency response performance the minimum allowed length is used. The width can be selected according to power handling capability. The physical layout of the device should minimize the input gate resistance.

The parameters under direct control of the designer are thus the number of stages, *n*, and the gate and drain inductance, L_g and L_d.[2] Hence for a given number of stages, there are only two parameters to vary. To achieve a good match to 50 Ω, one generally chooses L_g and L_d to set the gate and drain impedances as close to 50 Ω as possible, limiting the range of values for these components tremendously. There seems to be only a single parameter *n* in the design of a distributed amplifier.

In practice one can trade gain for bandwidth by increasing the gate and drain cutoff frequencies through adding a series capacitor to the gate of the input stages. The design tradeoff must be evaluated carefully, though, since a lower gain with more bandwidth can also be achieved by simply reducing *n*. In Fig. 13 we plot the value of gain versus frequency for the FET-217 transistor (*n*=4) using the gate and drain line parameters given in (13). Also plotted is the

[2] To extend the frequency response, coupled inductors in the form of *T*-coils may be employed [7]. This topology has a cutoff frequency √`2 times higher than the topology analyzed in this paper.

expression for gain derived by [3]. The deviation of ideal flat behavior is actually mostly due to the non-constant image impedance. This is why the *m*-derived matching network is necessary. In Fig. 13 we also show the gain for a matched design. Note that the matching network improves the gain flatness and is a critical part of the distributed amplifier.

Also evident from (25) is the strong dependence on the gate and drain attenuation factors. As discussed before, the attenuation factors in fact set the optimum number of stages for gain. Naively, the gain should increase as we add stages, as shown by the approximate expression of [5] where n^2 dependence is shown. But eventually the attenuation on the gate line will drive the input voltage to negligibly small values and adding further stages will simply increase the length and hence attenuation on the drain line without contributing to the output current. This is shown in Fig. 14, where the gain at 2 GHz is plotted as a function of *n* (a low frequency is selected so that the effects of gain roll-off will not come into play). The optimum number of stages may be calculated from evaluating the derivative of (25) with respect to *n*

$$n_{opt} = \frac{\ln \frac{a_d}{a_g}}{a_d - a_g} \tag{26}$$

The above expression is frequency dependent and may be evaluated to optimize the low frequency gain. Otherwise, we may use effective average values of the propagation loss factors

$$\overline{a} = \frac{1}{w_c}\int_0^{w_c} |a(w)|dw \tag{27}$$

C. Actively Loaded Gate Line

The above analysis identifies the attenuation loss factors as the main design constraint in achieving large values of gain by limiting the number of practical stages one can employ. In a modern CMOS process, these factors are the dominant limiting factors since high Q passive devices are difficult to implement due to the conductive substrate.

To boost the AC gain at the expense of DC power, the circuit topology of Fig. 15 may be used. For stability, the negative resistance must be chosen so that the total real impedance has a positive real part at all frequencies of interest. In practice, it will be difficult to achieve a constant negative resistance over a broad range of frequencies. This is not a big limitation since the frequency dependence of the –R stage can help overcome the frequency dependence in α.

In Fig. 16 we plot the gate loss with and without the –R stage. The reduction in the attenuation loss is clear. The design equations for the actively loaded gate transmission line are the following along with (4) and (5)

$$Z_1 = r_x + jwL \tag{28}$$

$$Y_2 = \frac{G_n + \frac{w^2}{w_g w_x}(G_n - G_x - G_i) + jw\left(\frac{2G_x - G_n}{w_x} + \frac{G_i - G_n}{w_g}\right)}{(1 + j\frac{w}{w_x})(1 + j\frac{w}{w_g})} \tag{29}$$

IV. Design Methodology

This section presents the systematic design procedure for distributed amplifiers introduced by Beyer et al. [3]. The amplifier analysis focuses on fundamental design considerations and establishes the maximum gain-bandwidth product for the distributed amplifier. The equations for gate and drain line attenuation can be rewritten in terms of normalized parameters

$$A_g = \frac{2aX_k^2}{n\sqrt{1 + \left[\frac{4a^2}{n^2} - 1\right]X_k^2}} \tag{30}$$

$$A_d = \frac{2b}{n\sqrt{1 - X_k^2}} \tag{31}$$

where

$$X_k = \frac{w}{w_c} \tag{32}$$

$$a = \frac{nw_c}{2w_g} \tag{33}$$

$$b = \frac{nw_d}{2w_c} \tag{34}$$

In the low-loss case, these expressions match the derivation of the previous sections as shown in Fig. 17. Using the above expressions, the normalized gain becomes

$$A_N = \frac{\sinh(\frac{b}{n})e^b \sinh h_- \exp(-h_+)}{\sinh(b)\left[1 + \frac{4a^2}{n^2}X_k^2\right]^{1/2}[1 - X_k^2]^{1/2}\sinh\frac{1}{n}h_-}$$

where

$$h_\pm = \frac{b}{\sqrt{1 - X_k^2}} \pm \frac{aX_k^2}{\sqrt{1 + \left(\frac{4a^2}{n^2} - 1\right)X_k^2}} \tag{35}$$

The gain, A_N is normalized to the low frequency gain

$$A_0 = \frac{g_m\sqrt{R_{o1}R_{o2}}\sinh(b)e^{-b}}{2\sinh(\frac{b}{n})} \tag{36}$$

where perfect impedance matching has been assumed.

From the equation (35) it is evident that the frequency response of the amplifier is completely determined by parameters *a* and *b* for a given number of stages *n*. The

values of *a* and *b* which give the same fractional bandwidth $X=f_{-1\mathrm{dB}}/f_c$ can be obtained by solving (35) numerically to find a frequency at which gain drops by 1 dB. Following the guidelines of [3], we have developed a non-linear equation solver for this purpose. Results for n=4 are shown in Fig. 18 where each curve in an *a*-*b* plane is plotted for a given value of *X*. The higher values of the fractional bandwidth occur for smaller values of *a*.

As shown in [5], the following expression can be derived from (36)

$$\frac{A_0 f_c}{4 f_{\max}} = \sqrt{ab}e^{-b} = K \tag{37}$$

where the maximum frequency of oscillation is given by

$$f_{\max} \cong \frac{g_m}{4pC_{gs}}\sqrt{\frac{R_{ds}}{R_i}} \tag{38}$$

Equation (37) may be written as

$$A_0 f_{1dB} = 4KXf_{\max} \tag{39}$$

and thus *KX* may be interpreted as gain-bandwidth product of the amplifier normalized to $4f_{\max}$. In order to explore tradeoffs in achieving maximum gain-bandwidth product we plotted curves of normalized low frequency gain *K* in the *a*-*b* plane in Fig. 19. One can see that higher values of *K* occur for higher values of *a*. This trend is opposite to the trend of an increase in *X* shown in Fig. 18. It is, therefore, evident that there exists a set of parameters *a* and *b* that maximizes the gain-bandwidth product. To determine these optimal values of *a* and *b* we have solved the problem of maximization of the gain-bandwidth product numerically. Curves of maximum gain bandwidth products are shown in Fig. 20 for n=2,4,6,8,12, where the maximum value of the product *KX*=0.2 is also indicated. It is interesting to note that the maximum gain-bandwidth product is the same for n=4,6,8,12 and it occurs for the same values of *a* and *b*. From the maximum value of *KX*=0.2 it follows that the maximum gain-bandwidth product is determined by the f_{max} of the device. It is given by

$$A_0 f_{1dB} \approx 0.8 f_{\max} \tag{39}$$

V. DISTRIBUTED AMPLIFIER NOISE FIGURE

The noise figure of a distributed amplifier is calculated in [8] assuming only Van der Ziel noise sources at the gate and the drain of an individual MESFET and lossless gate and drain transmission lines. The equivalent gate and drain current noise generators are given by

$$\bar{i}_g^2 = 4kT_0 B\frac{w^2 C_{gs}^2}{g_m}R \tag{42}$$

$$\bar{i}_d^2 = 4kT_0 B g_m P \tag{43}$$

where *R* and *P* are numerical factors in a Van der Ziel noise model. In order to calculate noise figure *F*, one has to account for noise sources associated with each transistor as well as noise sources due to gate and drain line terminations. The noise figure *F* is given by [8]

$$F = 1+\left(\frac{\sin nb}{n\sin b}\right)^2 + \frac{4}{n^2 g_m^2 R_{01}R_{02}} + \frac{R_{01}w^2 C_{gs}^2 R\sum_{r=1}^{n} f(r,b)}{n^2 g_m} + \frac{4P}{ng_m R_{01}} \tag{40}$$

where

$$f(r,b) = (n-r+1)^2 + \left(\frac{\sin(r-1)b}{\sin b}\right)^2 + \frac{2(n-r+1)\sin(r-1)b\cos rb}{\sin b} \tag{41}$$

It is worthwhile to examine various terms in the expression for the noise figure. The second and third term in (40) arise due to gate and drain line terminations, respectively, and can be made small by increasing *n*. The fourth term, which is due to gate generators contains a summation over all transistors (41). Forward and reverse amplifications of the gate noise current of the *r-th* transistor give rise to first and second terms in the expression for *f(r,b)* (41), whereas the interference between two amplification paths results in a third term in (41). The last term in (40) is due to the drain current generators.

VI. SAMPLE 4-STAGE DESIGN

Based on the design procedure of section IV and V, we have designed a 4-stage distributed amplifier using the FET-217 transistor. In order to achieve the maximum gain bandwidth product we have chosen an operating point in the *a*-*b* plane that results in a maximum gain-bandwidth product as demonstrated in Fig. 20. At this point *a*=0.375 and *b*=0.25. The same values of *a* and *b* need to be achieved from definitions of *a* and *b* given in (33) and (34). Multiplying (33) by (34), one finds

$$ab = \frac{n^2 w_d}{4w_g} = 4\frac{R_i C_{gs}}{R_{ds}C_{ds}} \tag{42}$$

which is a parabola in the *a*-*b* plane. The intersection of this parabola with a maximum gain-bandwidth curve defines a design point in the *a*-*b* plane. A location of the parabola in the *a*-*b* plane can be adjusted by placing the capacitor C_p in parallel to C_{ds} of a MESFET and thus increasing the overall C_{ds} that enters equation (42). To achieve the optimal design, the parabola (42) has to intersect the maximum gain-bandwidth curve at *a*=0.375, *b*=0.25, as shown in Fig. 21. This procedure determines the optimal value of C_p=0.16pF. If C_p is less than the optimal value, then the gain-bandwidth product is lowered by the excessive value of the drain inductance needed. If the C_p is greater than the optimal value, then the excessive value of C_{ds} limits the gain-bandwidth product. From equations (33), (34) and the condition of equal phase velocities along gate and drain lines we find required values of line inductors L_g=1.983nH and L_d=2.386nH, which result in f_c=12.9GHz. Gate and drain lines characteristic impedances are R_{01}=79.7 and

R_{02}=95.7 respectively. Predicted values of voltage gain and 1dB bandwidth are 14dB and 10GHz, respectively.

The schematic diagram of the 4-stage design is shown in Fig. 22. Simulated gain and input match performances are demonstrated in Fig. 23, where the gate to drain capacitance C_{gd} set to zero in all MESFETs. Design predictions and simulation results are in excellent agreement. However, the drain to gate capacitance C_{gd}=30 fF is a parasitic element present in the device model and can not be neglected or reduced. Simulations with C_{gd} included are shown in Fig. 24 where one can clearly see a strong resonance peak near the cutoff frequency seriously degrading the gain flatness.

The gain flatness can be restored by properly adjusting the *m*-derived matching sections at the gate and drain lines. In a practical design it is also beneficial to eliminate matching transformers at gate and drain terminations and match the transmission lines to 50 directly. In order to realize these goals, we have used the HP EE-Sof optimization routine to vary component values of the *m*-derived matching sections and to optimize the design for a 1dB gain flatness in a 1 to 10 GHz frequency band. The resulting circuit schematic is shown in Fig. 25. Results of the optimization are presented in Fig. 26(a) together with portions of S_{11} curves for non-optimized and ideal designs. The 1dB gain flatness can be achieved in a 1.8 to 10 GHz band at the expense of the gain degradation from 14.5 dB to 12.5 dB. Frequency dependence of S_{11} and S_{21} in a wider band, up to 15 GHz, is shown in Fig. 26(b).

Noise performance of the distributed amplifier has been investigated using Van der Ziel noise model of a MESFET. The noise figure has been calculated as a function of frequency for several optimized designs with different number of stages. We have chosen Van der Ziel parameter values, R=0.2 and P=0.6, in accordance with [8]. Results are presented in Fig. 27 for 4- and 6-stage designs. The noise figure for both designs increases at low and high frequencies, which corresponds to β approaching 0 and π, respectively. This behavior results in development of a minimum in noise figure at a certain frequency. Comparison of 4- and 6-stage design allows us to make an observation that the noise figure is lower for a higher number of stages. Furthermore, it can be shown [8] that in the limit of large n there exists an optimal value of n resulting in a minimum noise figure. In this project, we have focused on a 4-stage design and minimized the average noise factor in the frequency band of interest with respect to the characteristic impedance of the gate line. The numerical optimization yielded optimal values of the characteristic impedance of the gate line of R_{01}=104.4 for a 4-stage design and R_{01}=118.9 for a 6-stage design. Noise figure curves corresponding to optimal values of R_{01} have been plotted in Fig. 27 and compared to non-optimized designs. It is evident from the Fig. 27 that optimized curves lie within a few tenths of a dB from the non-optimized ones. Therefore, we conclude that the design procedure for a maximum gain-bandwidth product results in a noise figure which is very close to the optimal value.

Simulation results of the noise figure using HP EE-Sof package are presented in Fig. 28. Frequency dependence of the noise figure is shown for an ideal design, a realistic design with C_{gd}=30 fF included, and an optimized design. Simulation results for the ideal case are in good agreement with predictions shown in Fig. 27. The design optimization for a 1 dB gain flatness results in the degradation of the noise figure by about 1dB.

VII. CONCLUSION

In this paper we have derived design equations for a distributed amplifier implemented with lossy passive components. We have also presented a design methodology in the low-loss case [3] and shown the design approach matches our predictions under the conditions of low loss. The noise figure of a distributed amplifier has also been investigated according to the work of [8]. Finally, a practical design has been performed and simulations match our design equations well. The importance of matching and optimization have also been illustrated for achieving ultimate gain flatness.

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