Dis 58 Indepth example of a design problem

Design? What is it → Choosing a circuit to accomplish a goal making

goal/behavior → cut.

Analysis: cut → behavior [volts/currents]

1. Understand behavior/goal we want to achieve
2. Formulate this as block diagrams/math
3. Think about limitations and constraints
4. Choose circuits and modify them
Noise cancelling headphones

1.6 How to get music signal to headphones
2.6 How to also add noise cancelling on top

Source resistance? There is no model of a clt

DAC

info (music)

10 voltage signal

DAC

+ source resistance

V_{DAC} ≤ 1V

fill this in

our clt to design

speaker

Goals

-1.5V ≤ V_{speaker} ≤ 1.5V

What do we have?

- Op amps (oo)
- Voltage sources (-1.5V)
- Resistors (oo)
\[ 0V \leq V_{DAC} \leq 1V \quad \rightarrow \text{centered at } \frac{1}{2}V \]

\[-1.5V \leq V_{\text{speaker}} \leq 1.5V \quad \rightarrow \text{centered at } 0V \]

max/min are source voltages

\[-\frac{1}{2}V \leq V_{DAC} - \frac{1}{2}V \leq \frac{1}{2}V \]

\[-\frac{3}{2}V \leq 3(V_{DAC} - \frac{1}{2}V) \leq \frac{3}{2}V \]

\[ V_{\text{speaker}} = 3(V_{DAC} - \frac{1}{2}V) \]

1. "Do the math"
2. Make a block diagram
3. Cuts for each block

Candidates for \(-\frac{1}{2}V_{\text{shift}}\)
- op amp
- tran resistance current, voltage
- now invert amp limitation
- voltage summer

\[ \frac{R_2}{R_1 + R_2} = 1? \]

CAn't make \(R_1\) or \(R_2 = 0\) if we want it to be useful
1. \[ 3 \left( V_{DAC} - \frac{1}{2}V \right) \leftrightarrow 3 V_{DAC} - \frac{3}{2}V \]

Implement \( \text{V or 2} \)

Design 1
- subtract \( \frac{3}{2}V \)
- multiply by 3

Not feasible
Why? Can't output higher than \(1.5V\)

Design 2
- Multiply by 3 \( \leftrightarrow \)
- subtract \( \frac{3}{2}V \)

\[ 0 \leq V_{DAC} \leq 1V \]
\[ 0 \leq 3V_{DAC} \leq 3V \]

\[ V_{DD} = 1.5V, \quad V_{SS} = -1.5V \]
\[-\frac{1}{2} \leq V_{DAC} - \frac{1}{2}V \leq \frac{1}{2}\]

\[V_1 = V_{DAC}\]

\[R_{th} = 50\ \Omega\ \text{(source resistance)}\]

\[\frac{V_{DAC}}{50\ \Omega} - \frac{1}{2}V = 0\]

\[1 - \hat{\gamma} = 0\]

\[\text{Subgoal: Find } R_2\text{ to center voltage}\]

\[\frac{V_{out}}{V_2} = \frac{V_{DAC}}{50\ \Omega} - \frac{1}{2}V = \frac{1}{2}V\]

\[-1.5V\]

\[\text{Make } V_2 = -1.5V\]

\[V_{out} = V_{DAC} \hat{\gamma} + \left(-\frac{3}{2}\right)(1-\hat{\gamma})\]

\[\text{Want to center at zero to not damage op-amp}\]

\[\text{Output } V_{out} = 0V\text{ when } V_{DAC} = \frac{1}{2}V\]

\[\frac{1}{2}V\text{ is the middle of } V_{DAC}\text{'s range}\]

\[\frac{3}{2} = 2\hat{\gamma}\]

\[\hat{\gamma} = \frac{3}{4}\]

\[\hat{\gamma} = \frac{3}{2} - \frac{3}{2}\]

\[\hat{\gamma} = \frac{3}{4}\]
\[ V_{V0} = \frac{R_2}{R_2 + 50\Omega} \]

\[ V^2 = 1 - \frac{1}{V} \]

\[ V_{DAC} = -\frac{1}{2} V \leq V_{DAC} \leq \frac{1}{2} V \]

\[ -1.5V \leq V_{DAC} \leq 1.5V \]

\[ \Rightarrow -1.5V \leq V_{out} \leq 1.5V \]

\[ V_{DAC} = (V) \]

\[ V_{out} = \alpha V_{DAC} + (1 - \alpha) (-1.5V) \]

\[ = \frac{V_{DAC}}{4} = \frac{3}{8} V \]

\[ V_{DAC} = 0V \]

\[ V_{out} = \frac{3}{4} \cdot 0V + \frac{1}{4} (-1.5V) \]

\[ = -\frac{3}{8} V \]

\[ \times \text{Amplify by 3} \cdot (\frac{1}{2} \rightarrow \frac{3}{2}) \]

\[ \Rightarrow \text{Amplify by 4} \cdot (\frac{3}{8} \rightarrow \frac{3}{2}) \]
Amplify by 4

\[ V_{\text{out}} = \left(1 + \frac{R_2}{R_1}\right) V_{\text{shift}} \]

Choose \( R_2 = 3R_1 \)

No loading at input terminal of non-inverting amp is an open (no current GPI#1)

Design done. No issues from source limitations.
Design goal:

\[ \text{heard} = \text{music} + \text{cancel} + \text{outside} \]

\[ \text{7 Want, cancel} = -\text{outside} \]

\[ \text{DAC} \rightarrow \text{new circuit} \rightarrow \text{speaker} \]

\[ \text{mic} \rightarrow \text{outside signal} \]

\[ \text{10dB} \]

\[ V_{\text{mic}} \]

\[ 0 \leq V_{\text{mic}} \leq 1 \]

\[ -\frac{1}{8} \leq V_{\text{cancel}} \leq \frac{1}{8} \]

\[ -\frac{1}{2} \leq V_{\text{mic}} - \frac{1}{2} V \leq \frac{1}{2} \]

\[ -\frac{1}{8} \leq -\frac{1}{4} (V_{\text{mic}} - \frac{1}{2} V) \leq \frac{1}{8} \]
\[ V_{\text{cancel}} = -\frac{1}{4} (V_{\text{mic}} - \frac{1}{2}V) \]

Voltage divider:

\[ V_{\text{mic}} \rightarrow \frac{1}{2} \rightarrow \frac{3}{8}V \text{ to } \frac{3}{8}V \]

\[ -1.8V \rightarrow \frac{1}{4} \]

\[ R_f = 10k\Omega \]

\[ R_2 = 30k\Omega \]

\[ \alpha = \frac{R_2}{R_1 + R_2} = \frac{30k}{40k} = \frac{3}{4} \]

\[ -\frac{3}{8}V \leq V \leq \frac{3}{8}V \]

- \frac{1}{8}V \text{ to } \frac{1}{8}V

Implement

\[ V_{\text{in}} \text{ to } V_{\text{out}} \]

\[ V_{\text{out}} = -\frac{R_2}{R_1} V_{\text{in}} \]

Can't just connect, need something.

Need an buffer.
Voltage summer
Disba (yesterday)
V_{out} = V_1 + V_2