1. Op-Amp Rules and Negative Feedback Rule

Here is an equivalent circuit of an op-amp (where we are assuming that $V_{SS} = -V_{DD}$) for reference:

(a) What are the currents flowing into the positive and negative terminals of the op-amp (i.e., what are $I^+$ and $I^-$)? Based on this answer, what are some of the advantages of using an op-amp in your circuit designs?

**Answer:**

The $u^+$ and $u^-$ terminals have no closed circuit connection between them, and therefore no current can flow into or out of them. This is very good because we can connect an op-amp to any other circuit, and the op-amp will not disturb that circuit in any way because it does not load the circuit (it is an open circuit).

(b) Suppose we add a resistor of value $R_L$ between $u_{out}$ and ground. What is the value of $v_{out}$? Does your answer depend on $R_L$? In other words, how does $R_L$ affect $A_{VC}$? What are the implications of this with respect to using op-amps in circuit design?

**Answer:**

Notice that $u_{out}$ is connected directly to a controlled/dependent voltage source, and therefore $v_{out}$ will always have to be equal to $A_{VC}$ regardless of what $R_L$ is connected to the op-amp. This is very advantageous because it means that the output of the op-amp can be connected to any other circuit (except a voltage source), and we will always get the desired/expected voltage out of the op-amp.

**For the rest of the problem, consider the following op-amp circuit in negative feedback:**
(c) Assuming that this is an ideal op-amp, what is $v_{\text{out}}$?

**Answer:**
Recall for an ideal op-amp in negative feedback, we know from the negative feedback rule that $u^+ = u^-$. In this case, $u^− = u_{\text{out}} = u^+$. 

(d) Draw the equivalent circuit for this op-amp and calculate $v_{\text{out}}$ in terms of $A$, $v_{\text{in}}$, and $R_L$ for the circuit in negative feedback. Does $v_{\text{out}}$ depend on $R_L$? What is $v_{\text{out}}$ in the limit as $A \to \infty$?

**Answer:**
Notice that the op-amp can be modeled as a voltage-controlled voltage source. Thus, we have the following equation:

$$v_{\text{out}} = A(v_{\text{in}} - v_{\text{out}})$$

$$v_{\text{out}} + Av_{\text{out}} = Av_{\text{in}}$$

$$v_{\text{out}} = v_{\text{in}} \frac{A}{1+A}$$

Thus, as $A \to \infty$, $v_{\text{out}} \to v_{\text{in}}$. This is the same as what we get after applying the op-amp rule. Notice that output voltage does not depend on $R$. Thus, this circuit acts like a voltage source that provides the same voltage read at $u^+$ without drawing any current from the terminal at $u^+$. This is why the circuit is often referred to as a “unity gain buffer,” “voltage follower,” or just “buffer.”

2. **An Inverting Amplifier**

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(a) Calculate $v_{out}$ as a function of $V_s$ and $R_1$ and $R_2$.

**Answer:**
Because the op-amp is in negative feedback, we know that $u^+ = u^- = 0V$. Therefore, $v_{out} = u^- - V_{R_2} = -I_{R_1}R_2$.

We also know that $I^+ = 0$, so $I_{R_1} = I_{R_2}$. Thus, $v_{out} = u^- - V_{R_2} = -I_{R_1}R_2 = -I_{R_1}R_2 = -V_s \frac{R_2}{R_1}$.

3. Charge Sharing

Consider the circuit shown below. In phase $\phi_1$, the switches labeled $\phi_1$ are on while the switches labeled $\phi_2$ are off. In phase $\phi_2$, the switches labeled $\phi_2$ are on while the switches labeled $\phi_1$ are off.

(a) Draw the polarity of the voltage (using + and − signs) across the two capacitors $C_1$ and $C_2$. (It doesn’t matter which terminal you label + or −; just remember to keep these consistent through phase 1 and 2!)

**Answer:**
One way of marking the polarities is + on the top plate and − on the bottom plate of both $C_1$ and $C_2$. Let’s call the voltage drop across $C_1$ $V_{C_1}$ and across $C_2$ $V_{C_2}$.

(b) Redraw the circuit in phase $\phi_1$ and phase $\phi_2$. Keep your polarity from part (a) in mind.

**Answer:**
Phase $\phi_1$

Phase $\phi_2$
(c) Find $V_{\text{out}}$ in phase $\phi_2$ as a function of $V_{\text{in}}$, $C_1$, and $C_2$.

**Answer:**

First, we must identify the floating node in phase $\phi_2$. For this circuit, the floating node is $u_3$, as we can see that charge on the “+” plates of $C_1$ and $C_2$ cannot flow to ground.

Now that we know what plates are connected to our floating node, we must find the charge on those plates in phase $\phi_1$. The two capacitors in series have a total capacitance of $C_{\text{eq}} = \frac{C_1 C_2}{C_1 + C_2}$. We know that there is a voltage of $V_{\text{in}}$ across this capacitor and thus $Q_{C_{\text{eq}}} = V_{\text{in}} \frac{C_1 C_2}{C_1 + C_2}$ charge. Because they’re in series, we know that the charge across the equivalent capacitance is the same as a charge across each individual capacitor. Since we are looking for the charge on the “+” terminals of those capacitors it will be:

$$Q_{u_3}^{\phi_1} = Q_{C_1} + Q_{C_2} = 2Q_{C_{\text{eq}}} = 2V_{\text{in}} \frac{C_1 C_2}{C_1 + C_2}$$

Similarly, we must find the charge on those plates in phase $\phi_2$.

$$Q_{u_3}^{\phi_2} = V_C C_1 + V_C C_2 = (u_3 - 0)C_1 + (u_3 - 0)C_2 = (V_{\text{out}} - 0)C_1 + (V_{\text{out}} - 0)C_2 = V_{\text{out}}(C_1 + C_2)$$

Because of the conservation of charge, we can equate the total charge in phase $\phi_1$ and phase $\phi_2$.

$$Q_{u_3}^{\phi_1} = Q_{u_3}^{\phi_2} \Rightarrow 2V_{\text{in}} \frac{C_1 C_2}{C_1 + C_2} = V_{\text{out}}(C_1 + C_2) \Rightarrow V_{\text{out}} = 2 \frac{C_1 C_2}{(C_1 + C_2)^2} V_{\text{in}}$$

(d) How will the charges be distributed in phase $\phi_2$ if we assume $C_1 \gg C_2$?

**Answer:**

We know that the capacitors are in parallel in phase $\phi_2$, so the voltage across both capacitors is the same. Considering that $Q = CV$, if $C_1 \gg C_2$, then $Q_1 \gg Q_2$. 