EECS 143 Microfabrication Technology

Lab Report 1

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Total Points = 110 possible (graded out of 100)

Please be sure to include the requirement signature regarding academic honesty. All lab group members should print out this page, sign on the attached form, and include it with your Lab Report. Thank you!

REPORTS MUST BE WORD PROCESSED (EXCEPT FOR SKETCHES AND HAND WRITTEN CALCULATIONS)

IF YOU MAKE AN ASSUMPTION, PLEASE STATE IT CLEARLY. PARTIAL CREDIT WILL BE GIVEN EVEN IF THE ANSWER IS NUMERICALLY WRONG.

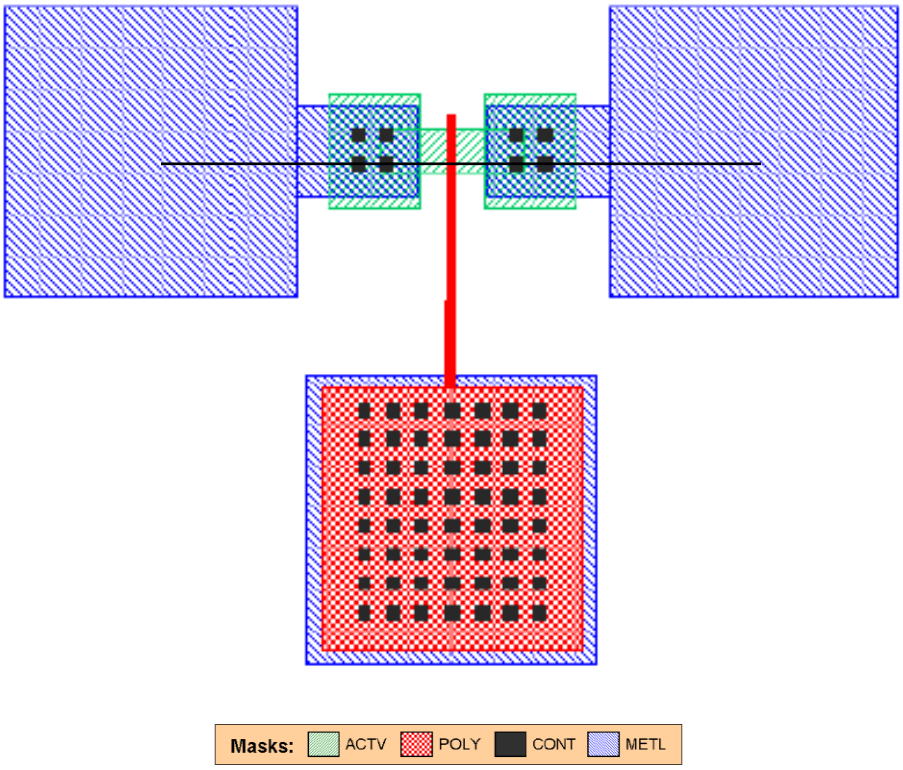
Each group of two students will submit one joint report. The report should be organized as follows:

1. **Profiles & Layout (9 Points)**

A. Draw cross-sectional profiles of a thin-oxide *MOSFET* (test structure 8) after each of the 11 major processing steps. Indicate all layers and specify important details such as the non-planar interfaces, isotropic etch profiles, point-source Al evaporation, thermal oxidation growth, etc. Label each feature and indicate thicknesses (make roughly proportional sketches). These drawings should have significantly more detail than those

on the lab manual website. See the diagram below for the exact cross-sections in question. (5 Points)

**Pay attention to details such as consumption of Si during oxidation and isotropic etching profiles and directional metal deposition.



B. Draw top views of the same thin-oxide *MOSFET* (test structure 8) after each of the four photolithography steps. (4 Points)

2. **Process Procedures (20 Points)**

A. List and concisely describe the problems occurred during the fabrication in the class (i.e., nonuniform film deposition, etc.). Specifically, these are the steps where all the wafers were run in batch (i.e. oxidation, poly-deposition, metallization). What were the sources of the problems, and how did you avoid them? Was there any process step during your lab section that deviated from the descriptions in the lab manual? If so, why were some steps done differently and how did it affect the outcome? How do you expect it to affect the performance/function of the device? (7 Points)

B. Other than the problems that occurred during the session, what were the particular problems (or deviations from the rest of the groups) that occurred in YOUR wafer? Specifically, these are the steps where all the wafers were run in individual processes (i.e.

photolithography, etch, etc.). What were the causes and how were the problems overcome? **Include any pictures/sketches that would be helpful**. (7 Points)

C. Describe monitoring measurements that were done during processing (color, line width, thickness, resistivity, etc.). Determine and describe whether and how much each layer was overetched or underetched? Did you purposely over/underetch? Why? How much each layer was misaligned to the neighboring layers? How much the misalignment acceptable in terms of the device function? **You may want to provide pictures taken to determine over/underetch and misalignment**. (6 Points)

We are looking to see that you understand how the process steps work.

3. **Calculations (36 Points)**

FOR CALCULATIONS, USE PROCESS CONDITIONS ENCOUNTERED DURING YOUR LAB SESSION.

Calculate the parameters asked for in the following questions—list both the theoretical values and the empirical values, when applicable. We would like to see that you understand what processing abnormalities may have led to a discrepancy between the two:

1. Theoretical and empirical thicknesses of field oxide, gate and intermediate oxides (Include orientation dependence of oxidation rate but not impurity dependence) (11 points)

2. Junction depths after pre-diffusion and drive-in (theoretical, assume only phosphorous doping with surface concentration limited by solid solubility) (12 points)

3. Final surface concentrations of dopants, as calculated using sheet resistance measurements made in lab. Plot of sketch the change of dopant profile after each thermal step. Label significant points such as peak concentration, peak width, junction depth, and show non-ideal effects such as dopant redistribution during oxidation (Field Ox, Gate Ox, Poly-Dep, Pre-Dep, Drive-In, Sintering) (6 points)

4. Lateral diffusion under the MOSFET gates. You may estimate, but provide justification for estimation. (theoretical) (4 points)

5. Draw a table with the following parameters from your own wafer summarizing your calculation (***example*** table attached at end of document): (3 points)

   a) Film Thickness (all layers)
   b) Sheet Resistance (ACTV after field oxidation, after S/D predeposition and drive-in, poly-Si)
   c) % Overetch/Underetch (all layers)

4. **Questions (35 Points)**

Answer these questions in the most concise manner possible. A few lines should suffice for each.

1. What type of photoresist (positive or negative? I-line or G-line?) do we use in the lab? Briefly describe how the resist responds to the process steps like spinning, UV light exposure and development. (2 points)

2. What is the purpose of baking the wafers at 120 °C before depositing HMDS? What is the purpose of the 90 °C bake after spinning on photoresist? What happens if the soft bake is too hot (say 150 °C)? (2 points)

3. What is the purpose of hard bake? What happens if we skip this step? What may happen if the bake is done at a temperature above 120 °C (say 150 °C)? (2 points)

4. We do lithography steps under yellow light only. What happens if we expose the wafers to fluorescent light before development? And after development? Would red light damage your process? (2 points)

5. What are the differences between wet and dry oxidation that lead us to use one for the gate oxide and one for the field oxide? What is the purpose of annealing in nitrogen after gate oxidation? (2 points)

6. How do you determine etching time using theoretical etch rate in literature? List two ways to determine etch time empirically from lab measurements, when you etch the layers. (Hint: these methods include visual cues.). How close are the experimental and the theoretically calculated values? (2 points)

7. Before n+ deposition (prior to SOG spinning), we clean in Piranha but not in HF. Before gate oxidation, we clean in both. Why the difference? (2 points)

8. Why is 5:1 BHF (5:1 NH_4F:HF) used for etching features in the oxide while 10:1 BHF is used for cleaning and p-glass stripping? Why buffered HF? (2 points)

9. What would happen if we skipped the HF dip before metallization? (2 points)

10. What is selectivity? What is the selectivity of HF between Si, oxide and PR? (2 points)

11. Why do we first use the roughing pump and then the turbomolecular pump when pumping down the aluminum deposition system? Why must the foreline pressure be kept below 100 mTorr? (2 points)

12. What is the Al etchant composed of? What happens if you use it at room temperature? What is the purpose of sintering? What will result if sintering step is skipped? What happens if sintering temperature is too hot or too low? (2 points)

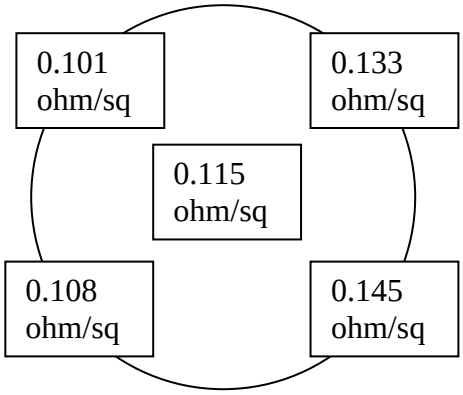
13. To characterize the gate oxidation furnace in the EE143 lab, the head TA performed three oxidation runs for different times while maintaining the same oxygen flow. The data obtained is below:

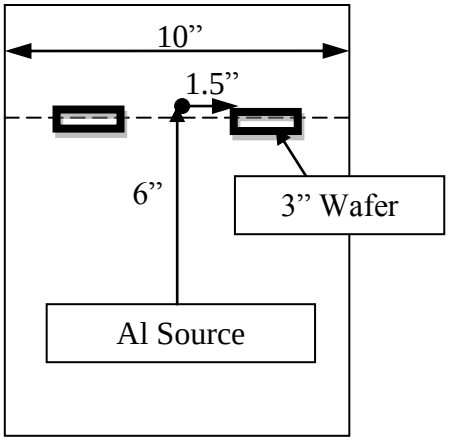
Oxidation Time (mins)	Oxide Thickness (angstroms)
40	1315
34	1181
25	1050

Using this data, how can the TA calculate the time needed to grow the desired 800 angstroms of gate oxide? (3 points)

14. Suppose that the normal poly-Si furnace we use to deposit in-situ phosphorus-doped poly was down for repair. There is another furnace that can be adapted to deposit poly-Si, but it can only deposit undoped and in-situ boron-doped films. How can we work around this problem and still obtain phosphorus-doped poly-Si with the methods and materials available to us in the EE143 lab? (4 points)

15. The head TA wanted to characterize the Al thickness uniformity in the Al evaporator used in the EE143 lab on an unpatterned Si wafer. Below is a wafer map labeled with the measured Al sheet resistances at those locations as well as a rough diagram of the Al evaporator dimensions. What was the average thickness of the Al film? How can the thickness pattern be explained and how can the thickness uniformity be improved? (4 points)





5. **Bonus Questions (up to 10 Points)**

(a) In class you learn about alternative methods for completing process steps (i.e. sputtering, LOCOS, etc.). Why do we not run these steps. Is there any benefit from using these methods in our lab? (5 points)

(b) What process steps would be different if you were making a PMOS device instead of NMOS? What additional steps would be involved to make complementary MOS (CMOS – both NMOS and PMOS on the same chip)? (5 points)

Updated on October 26, 2010 by Byron Ho

EECS 143 Lab Report 1

Fall 2010

In signing below, I attest to the fact that I have read and have adhered to the policies and guidelines discussed in the EECS Departmental Policy on Academic Dishonesty, as found at: http://inst.eecs.berkeley.edu/~ee143/fa10/policy.html

Name 1: _____

Signature: _____

Date:_____

Name 2: _____

Signature: _____

Date:_____

Name 3: _____

Signature: _____

Date:_____

Film Thicknesses:

Layer	*Theoretical Calculation*	*Experimental (Nanospec)*	*Experimental (Etch Time)*	*% Error from theoretical (Nanospec)*	*% Error from theoretical (Etch Time)*	*Measured Linewidths*				*% Overetch (Linewidths)*			
						2	*3*	*4*	*8*	*2*	*3*	*4*	*8*
Field Oxide													
Polysilicon													
Gate Oxide													
Intermed Oxide													
Aluminum													

Overetch:

Layer	*Measured Thickness before etch*	*Theoretical Etch Time*	*Actual Etch Time*	*% Overetch of thickness*	
Field Oxide					
Polysilicon					
Gate Oxide					
Intermed Oxide					
Aluminum					

Sheet Resistance:

Layer	*Sheet Resistance*	*Surface Concentration (Calculated)*
ACTV After Field Oxidation		
Polysilicon		
ACTV After Pre-Dep		
ACTV After Drive-in		

Calculated Junction Depths

Layer	*Vertical Junction Depth*	*Lateral Junction Depth*
ACTV After Pre-Dep		
ACTV After Drive-in		