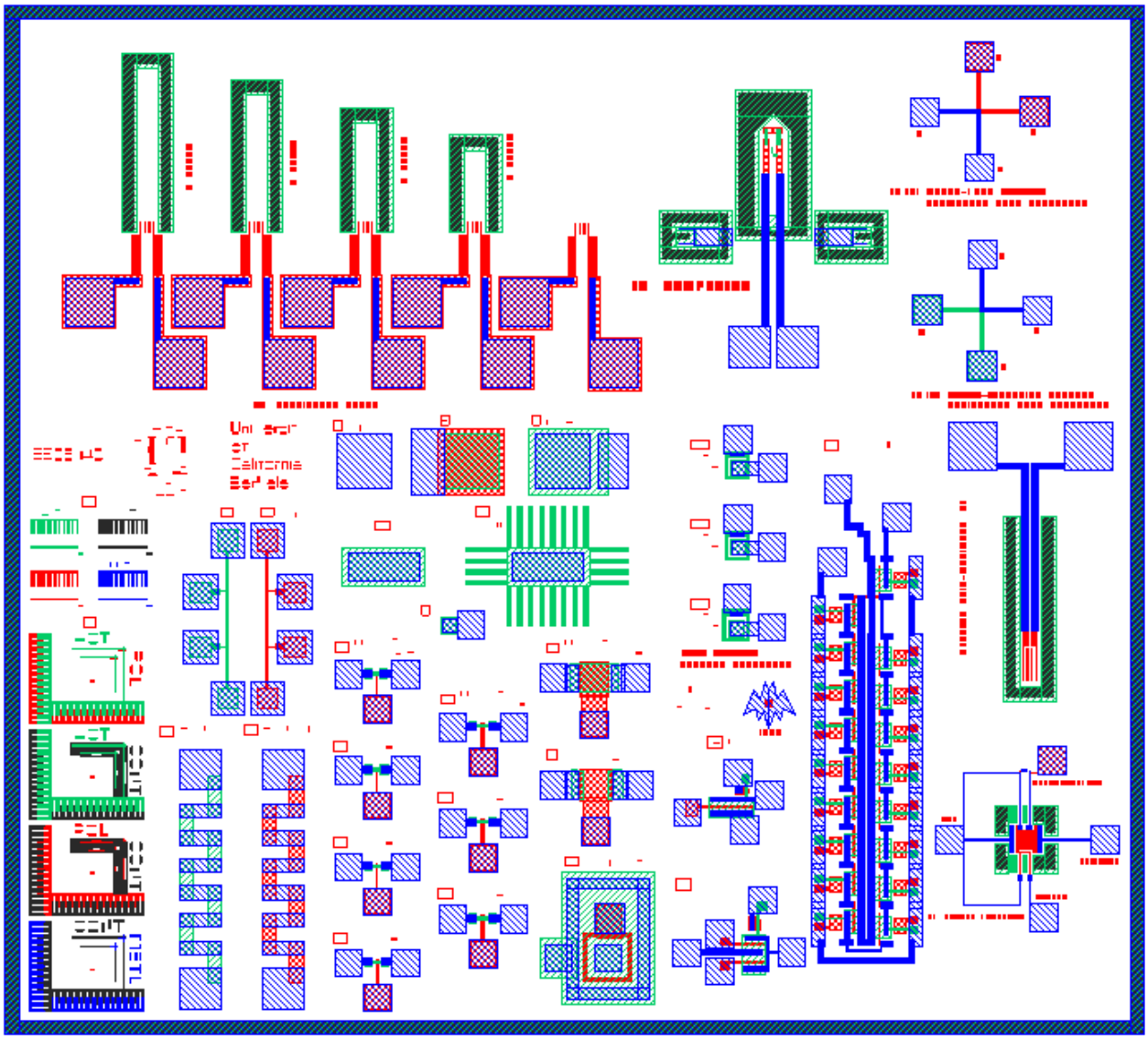
EECS 143
Microfabrication
Technology

Chip Layout:



Device Sizes:

Layout dimensions dimensions are in micrometers (1 µm = 1 micrometer). All contact holes are 5 µm x 5 µm. Metal pads are 100 µm x 100 µm. The devices are listed below by device number:

1a) Resolution Test Patterns (1 per mask):

Line widths as marked: 2, 3, 4, and 8 µm

Rails: 10 µm

1b) Alignment Marks and Verniers:

Vernier steps: 0.2 µm

2a) Diffused Resistor:

20 squares (L = 200 µm, W = 10 µm)

2b) Poly Resistor:

20 squares (L = 200 µm, W = 10 µm)
2c) Metal-to-Diffusion Contact Chain:
14 contacts. Diffused segments: L = 150 µm x W = 50 µm
2d) Metal-to-Poly Contact Chain:
14 contacts. Diffused segments: L = 150 µm x W = 50 µm
3) Field Oxide Capacitor:
Top Metal Plate: 200 µm x 200 µm
4) Gate Oxide Capacitor:
Active Area: 200 µm x 200 µm
Top Plate (poly): 240 µm x 240 µm
Metal Contact Pad (not including metal-poly overlap): 95 µm x 240 µm
5) Intermediate Oxide Capacitor:
Top Metal Plate: 200 µm x 200 µm
6a) Junction Capacitor:
Active Area: 300 µm x 140 µm
6b) Long Periphery Junction Capacitor:
Center of Active Area: 300 µm x 140 µm
Fins: 150 µm x 20 µm
7) Diode:
Active Area: 50 µm x 50 µm
8) MOSFETs of various lengths:
W/L = 15/4, 15/6, 15/8, 15/10 µm
9) Long Channel MOSFETs:
W/L = 10/20, 15/20, 20/20 µm
10) Large MOSFET:
W/L = 100/100 µm
11) Field Oxide MOSFET:
W/L = 100/100 µm
12) Circular MOSFET:
W/L = ~560/20 µm
13) Lateral BJTs
Base Widths = 5, 7, 9 µm
Emitter Dimensions (Active Area): 50 µm x 50 µm
14) Inverter:
Load: W/L = 10/20 µm
Driver: W/L = 80/10 µm
15) NOR Gate:
Load: W/L = 10/20 µm
Driver: W/L = 80/10 µm
16) Ring Oscillator (17 stages + buffer):
Load: W/L = 10/20 µm
Driver: W/L = 80/10 µm

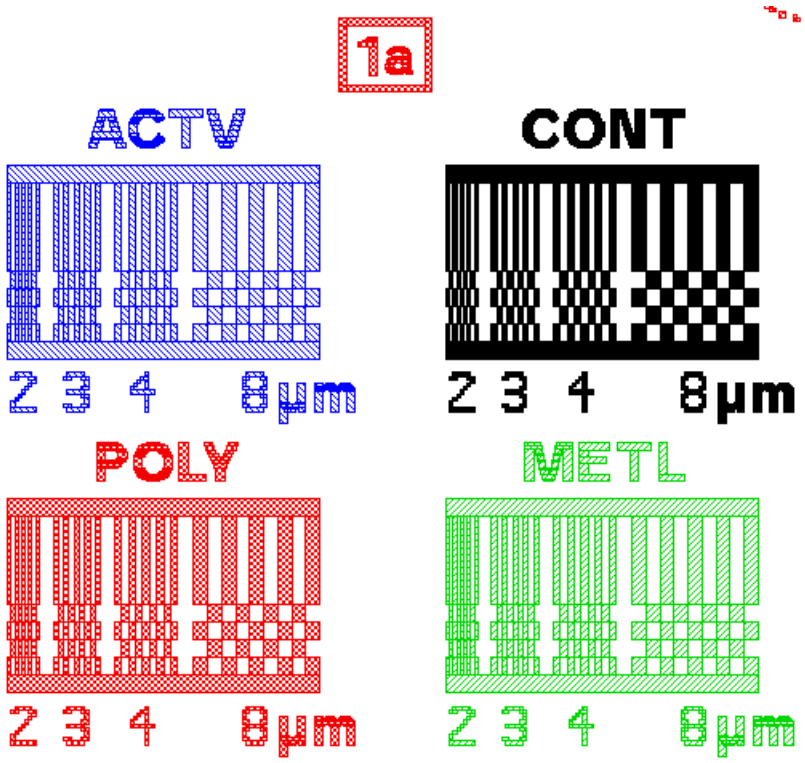
For MEMS Layout, check the MEMS Chip Layout Page

Initials of the designers

Resolution Test Pattern Layout:

1) Resolution Test Patterns (1 per mask):

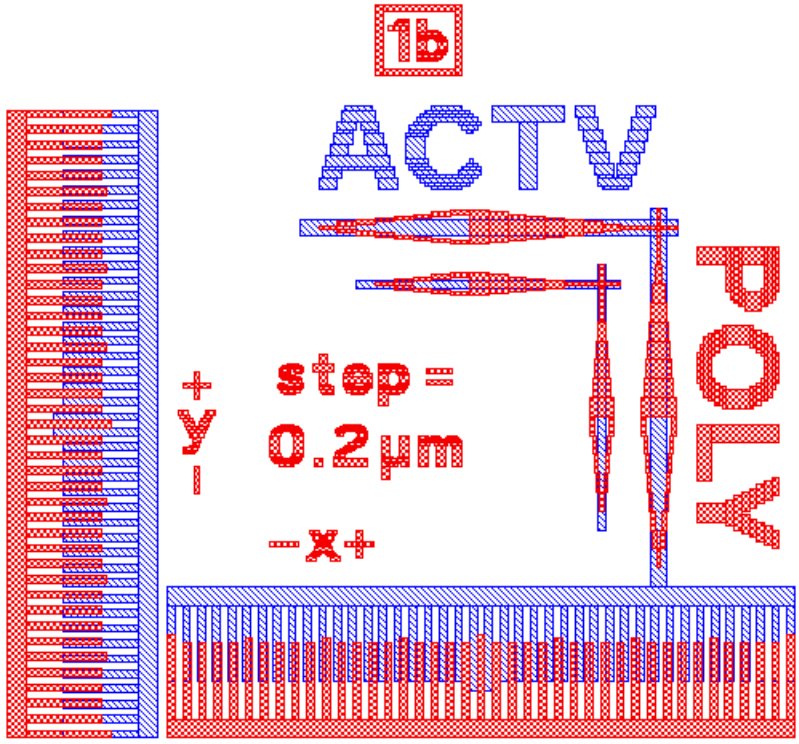
Line widths as marked: 2, 3, 4, and 8 µm
Rails: 10 µm

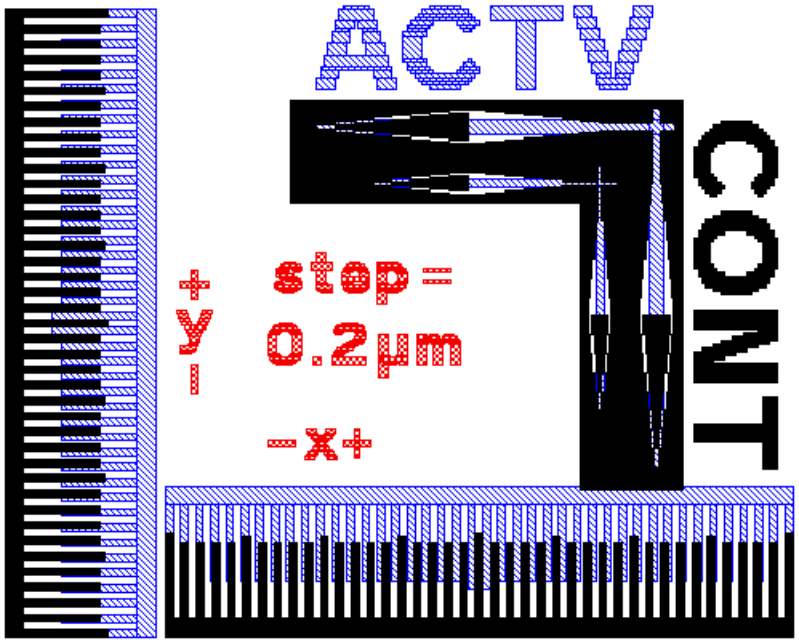


Alignment Marks and Vernier Layout

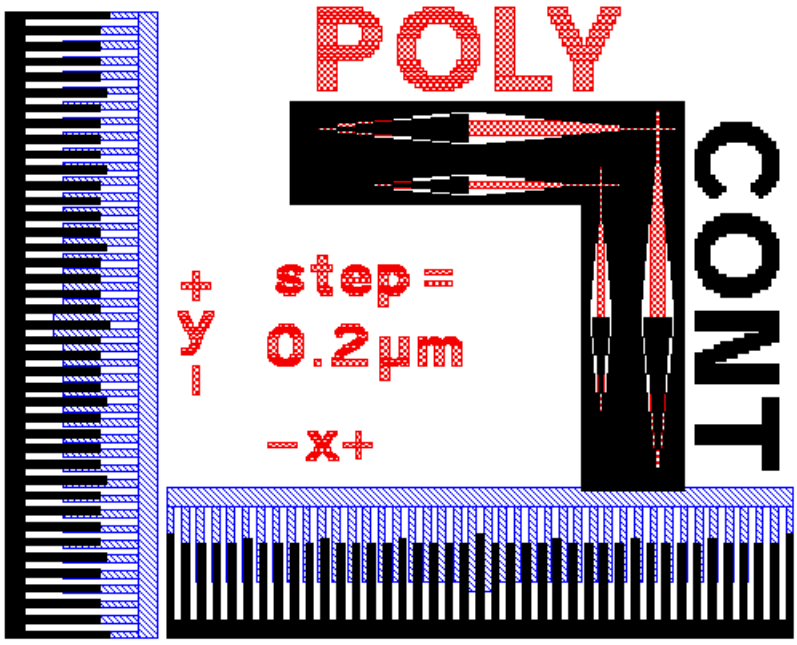
1b) Alignment Marks and Verniers:

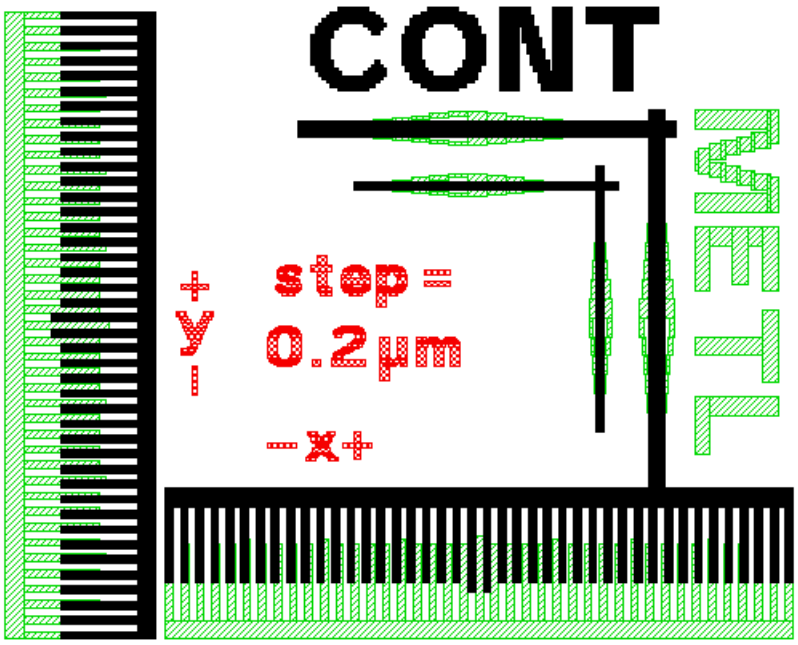
Vernier steps: 0.2 µm





1b continued





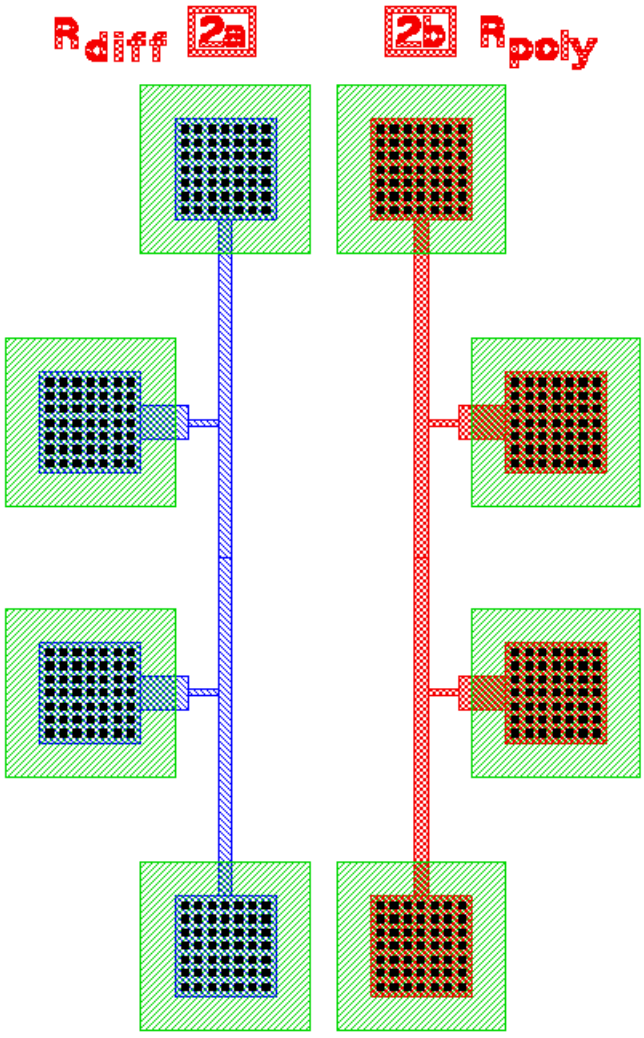
Resistor Layout:

2a) Diffused Resistor:

20 squares (L = 200 µm, W = 10 µm)

2b) Poly Resistor:

20 squares (L = 200 µm, W = 10 µm)



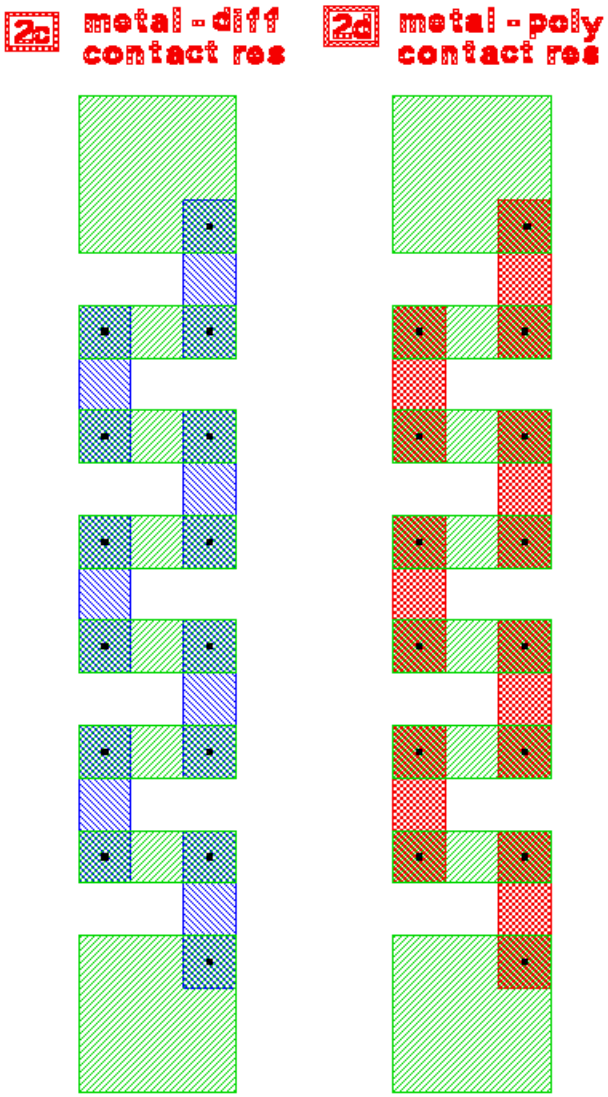
Contact Chain Layout:

2c) Metal-to-Diffusion Contact Chain:

14 contacts. Diffused segments: L = 150 µm x W = 50 µm

2d) Metal-to-Poly Contact Chain:

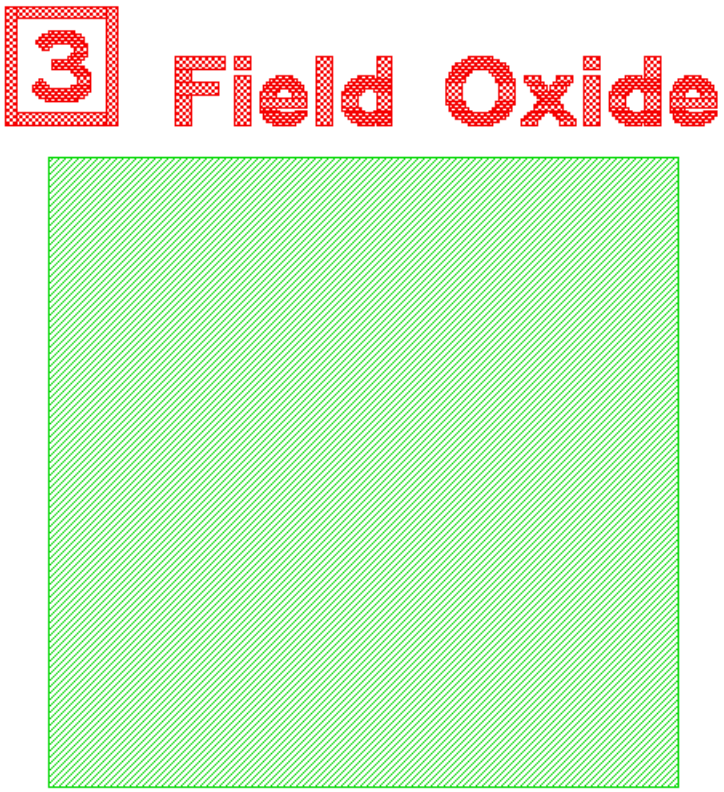
14 contacts. Diffused segments: L = 150 µm x W = 50 µm



Field Oxide Capacitor Layout:

3) Field Oxide Capacitor:

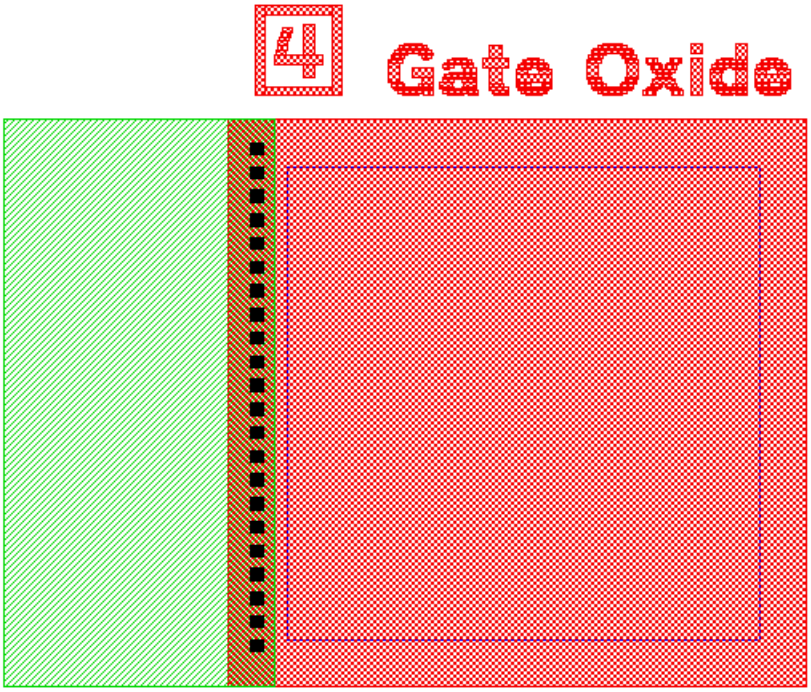
Top Metal Plate: 200 µm x 200 µm



Gate Oxide Capacitor Layout:

4) Gate Oxide Capacitor:

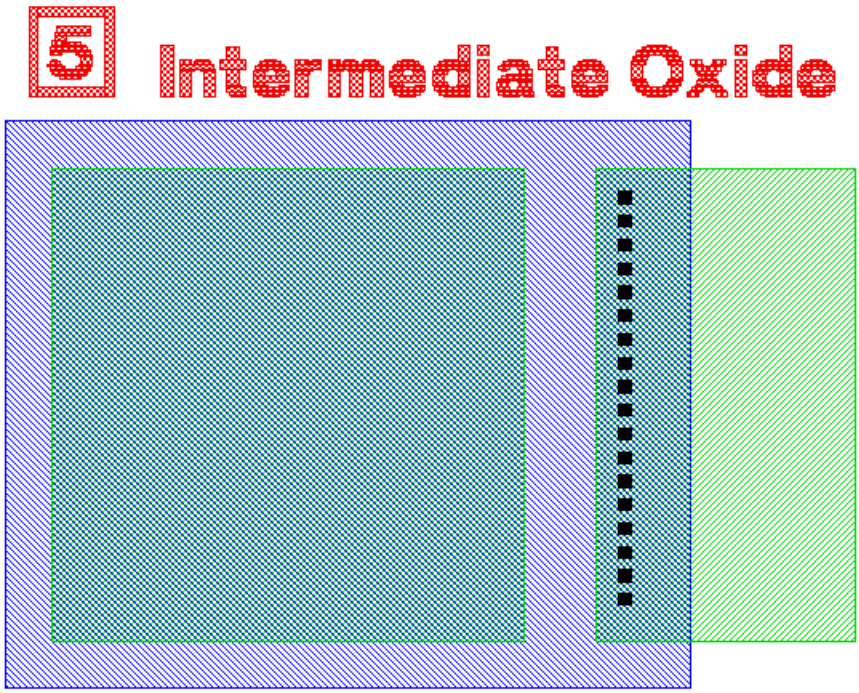
Active Area: 200 µm x 200 µm
Top Plate (poly): 240 µm x 240 µm
Metal Contact Pad (not including metal-poly overlap): 95 µm x 240 µm



Intermediate Oxide Capacitor Layout:

5) Intermediate Oxide Capacitor:

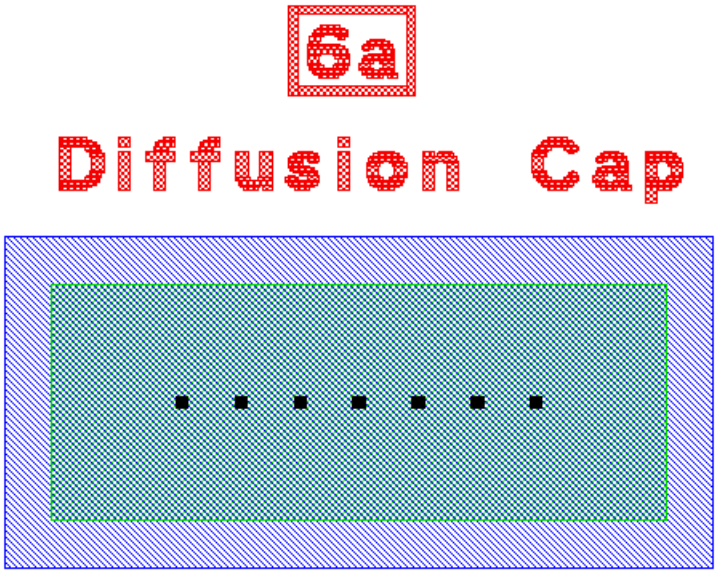
Top Metal Plate: 200 µm x 200 µm



Junction Capacitor Layout:

6a) Junction Capacitor:

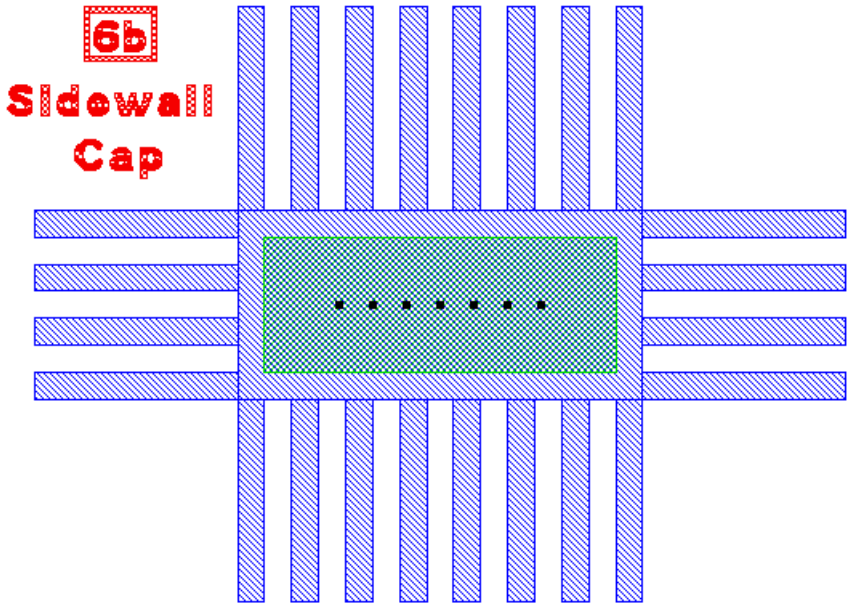
Active Area: 300 µm x 140 µm



Long Periphery Junction Capacitor Layout:

6b) Long Periphery Junction Capacitor:

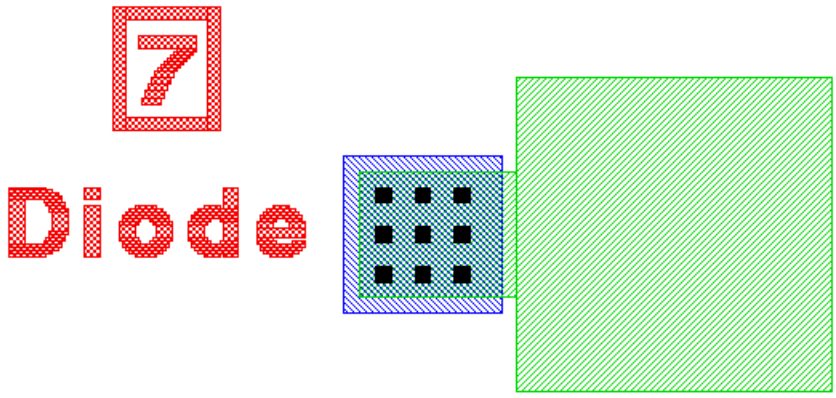
Center of Active Area: 300 µm x 140 µm
Fins: 150 µm x 20 µm



Diode Layout:

7) Diode

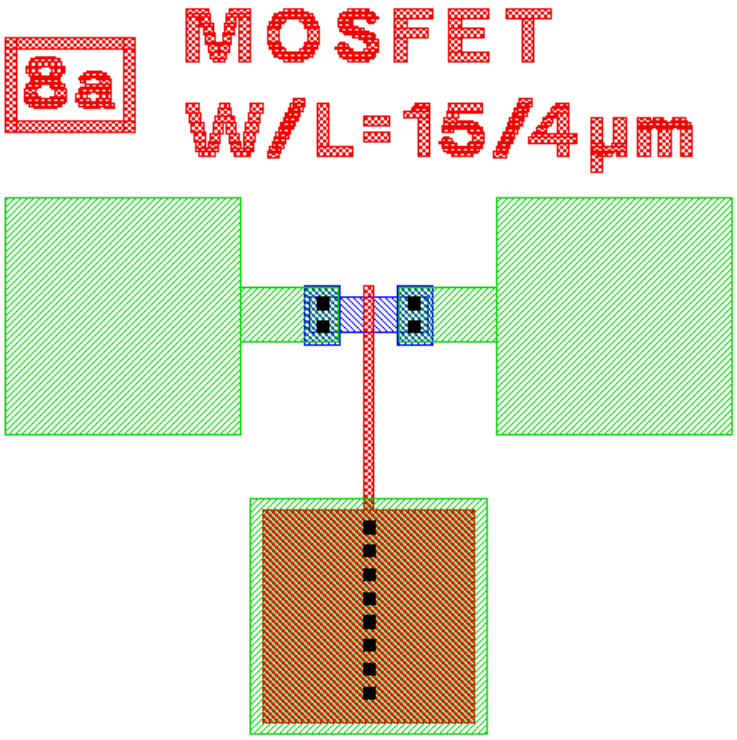
Active Area: 50 µm x 50 µm

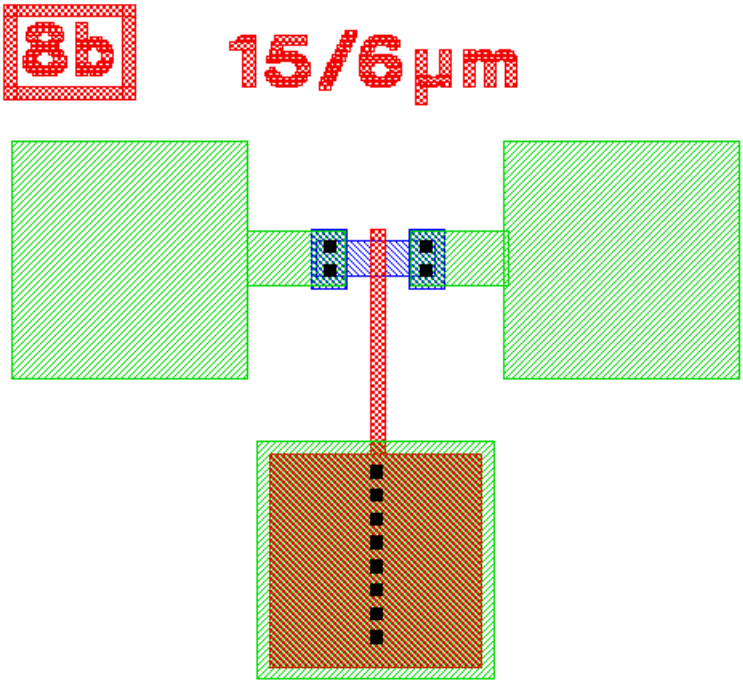


MOSFETs of Various Lengths Layout:

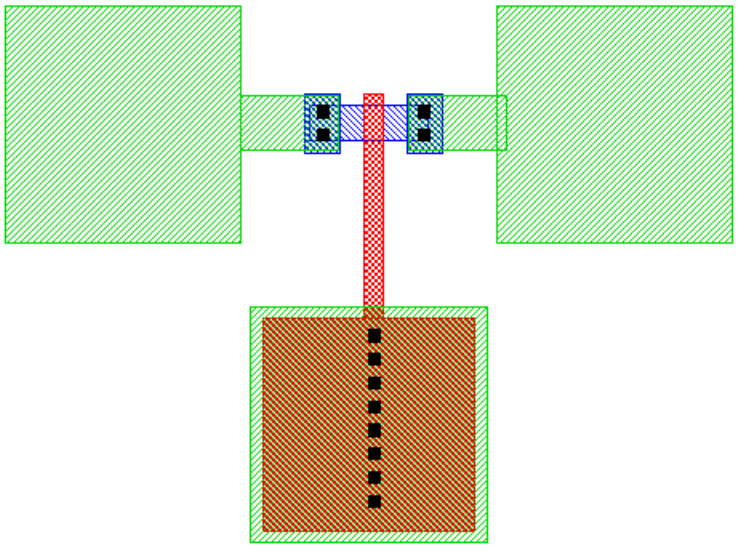
8) MOSFETs of various lengths:

W/L = 15/4, 15/6, 15/8, 15/10 µm

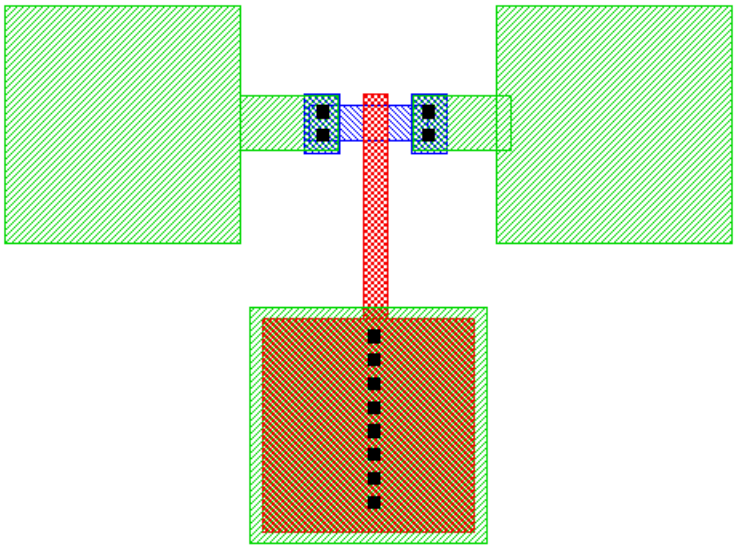




8c 15/8µm



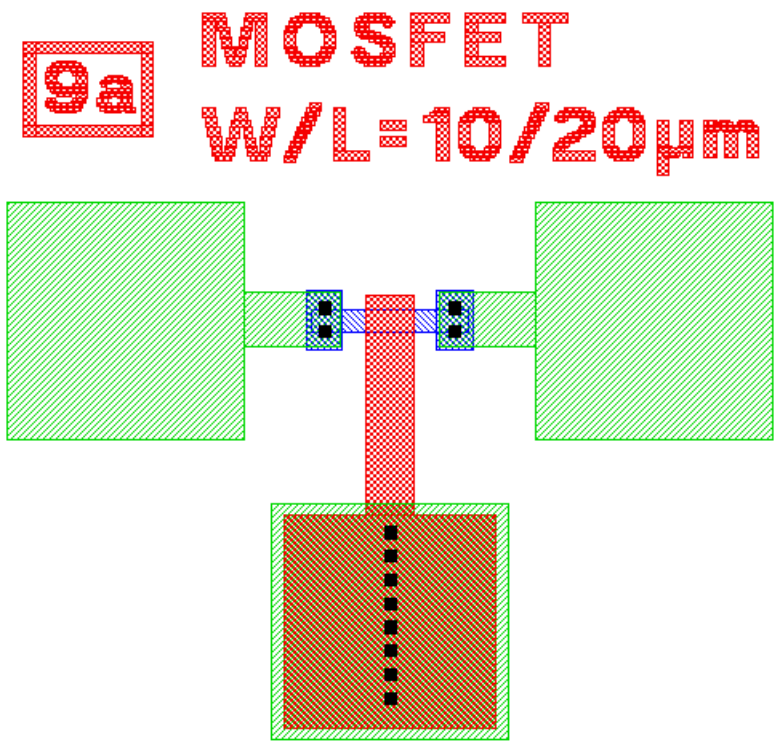
8d 15/10µm

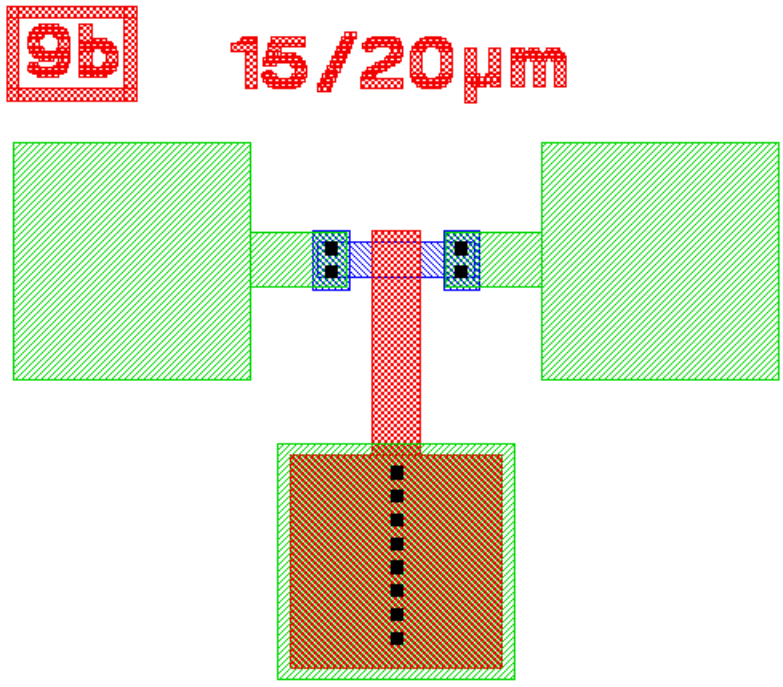


Long-Channel MOSFETs of Various Widths Layout:

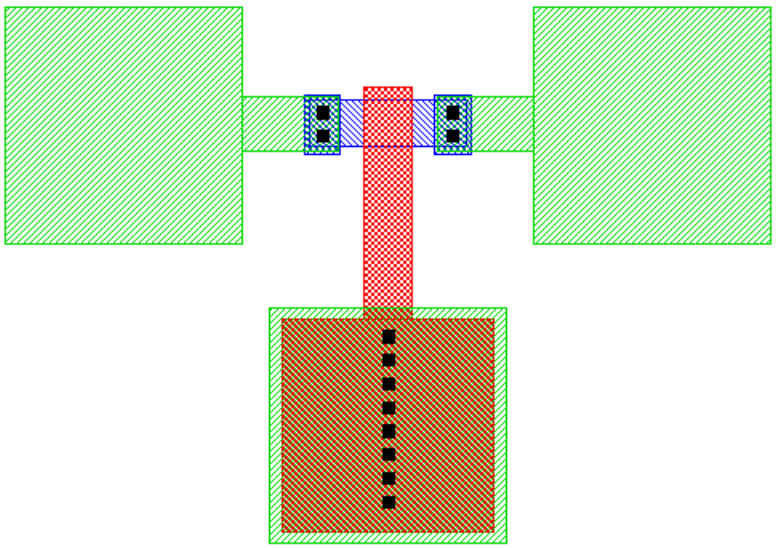
9) Long Channel MOSFETs:

W/L = 10/20, 15/20, 20/20 µm





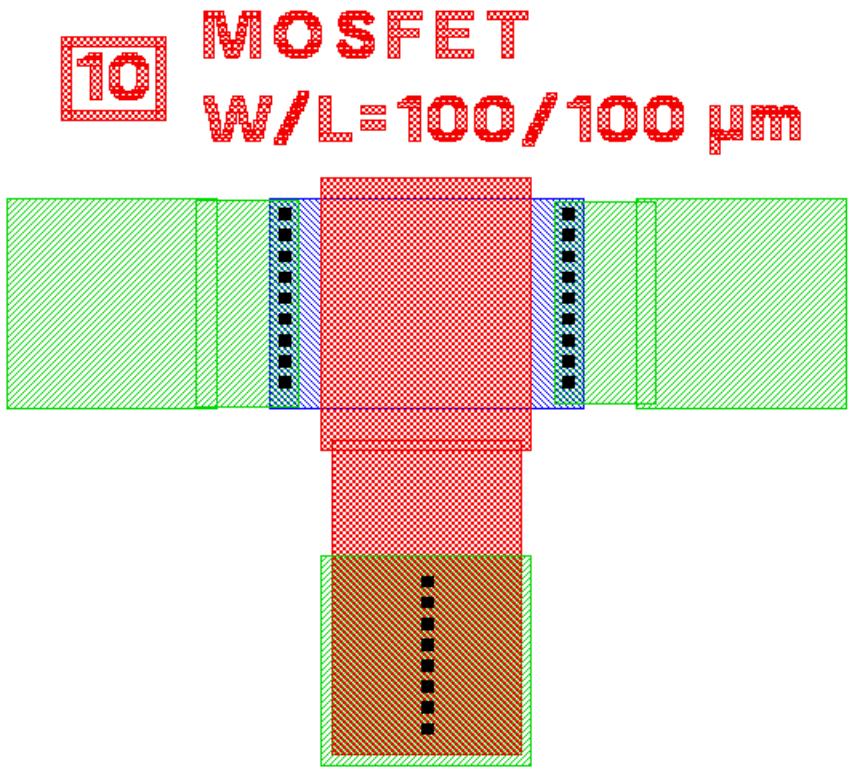
9c 20/20µm



Large-Area MOSFET Layout:

10) Large MOSFET:

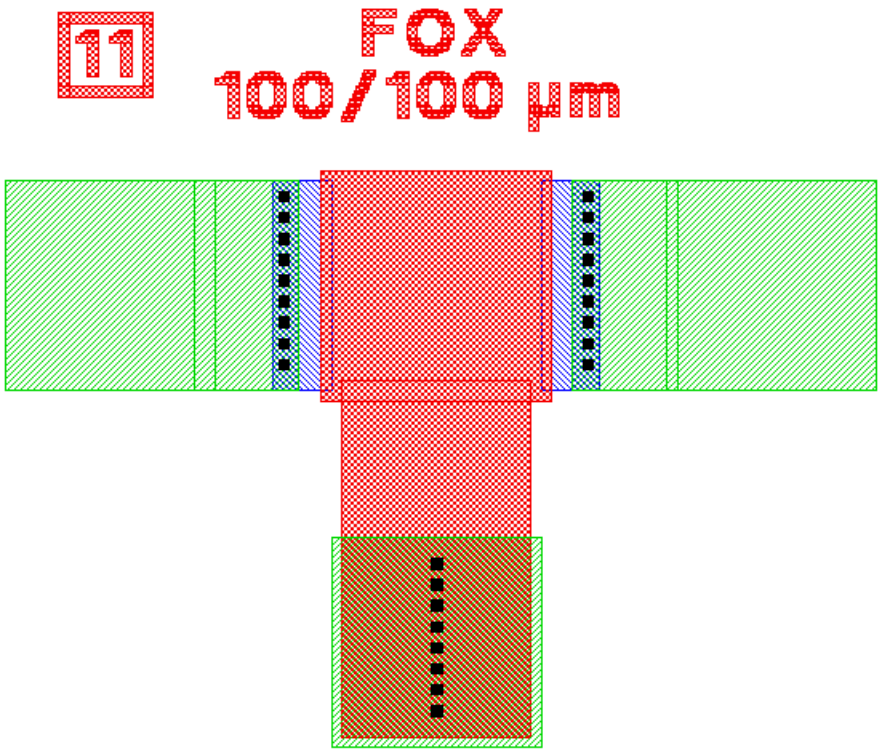
W/L = 100/100 µm



Field Oxide MOSFET Layout:

11) Field Oxide MOSFET:

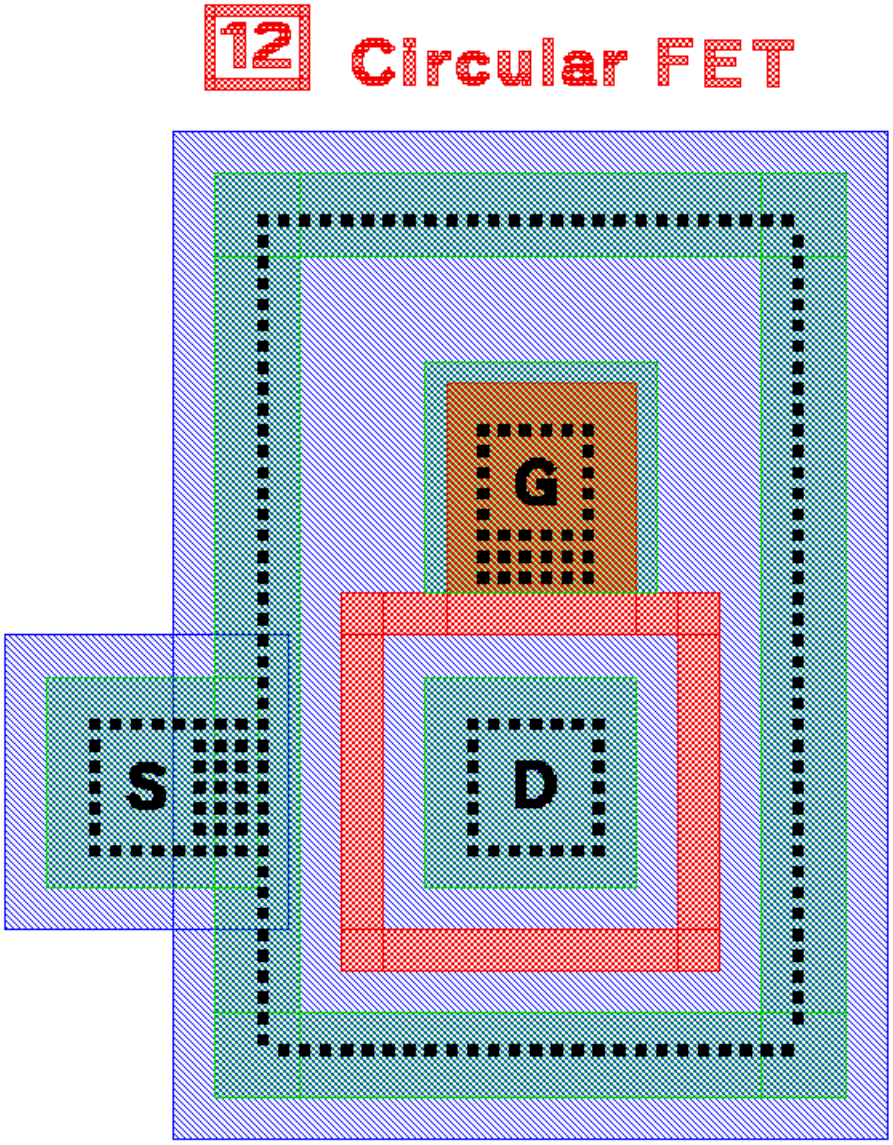
W/L = 100/100 µm



Circular MOSFET Layout:

12) Circular MOSFET:

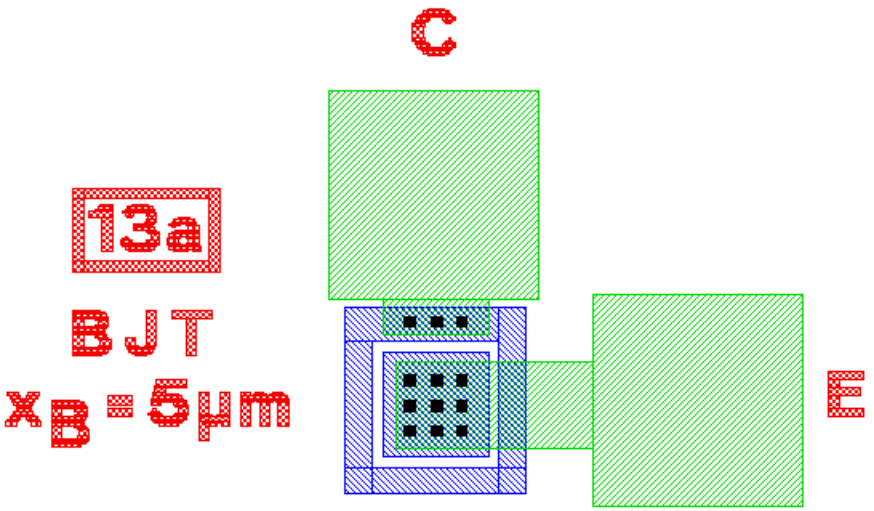
W/L = ~560/20 µm

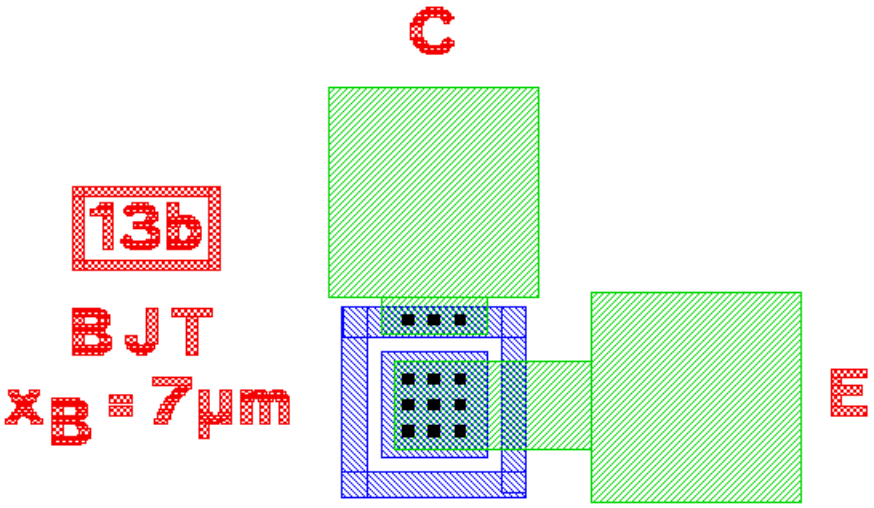


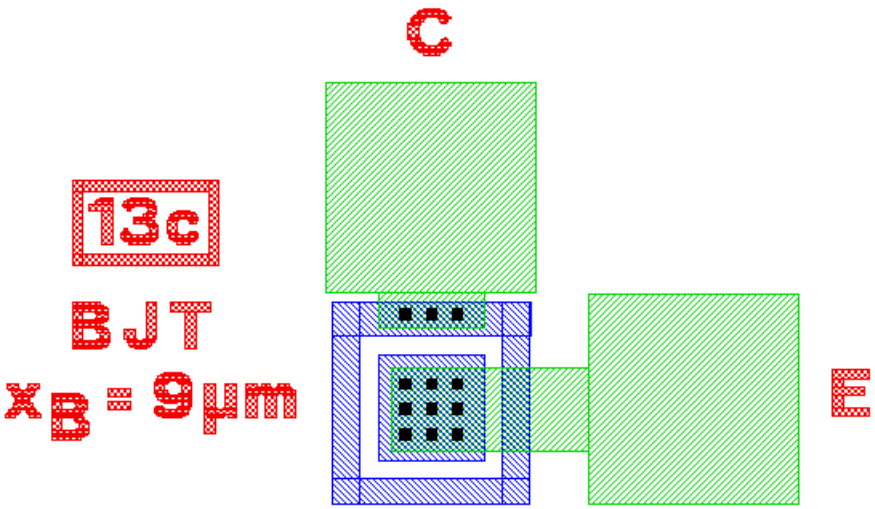
Lateral BJT Layout:

13) Lateral BJT's

Base Widths = 5, 7, 9 µm
Emitter Dimensions (Active Area): 50 µm x 50 µm



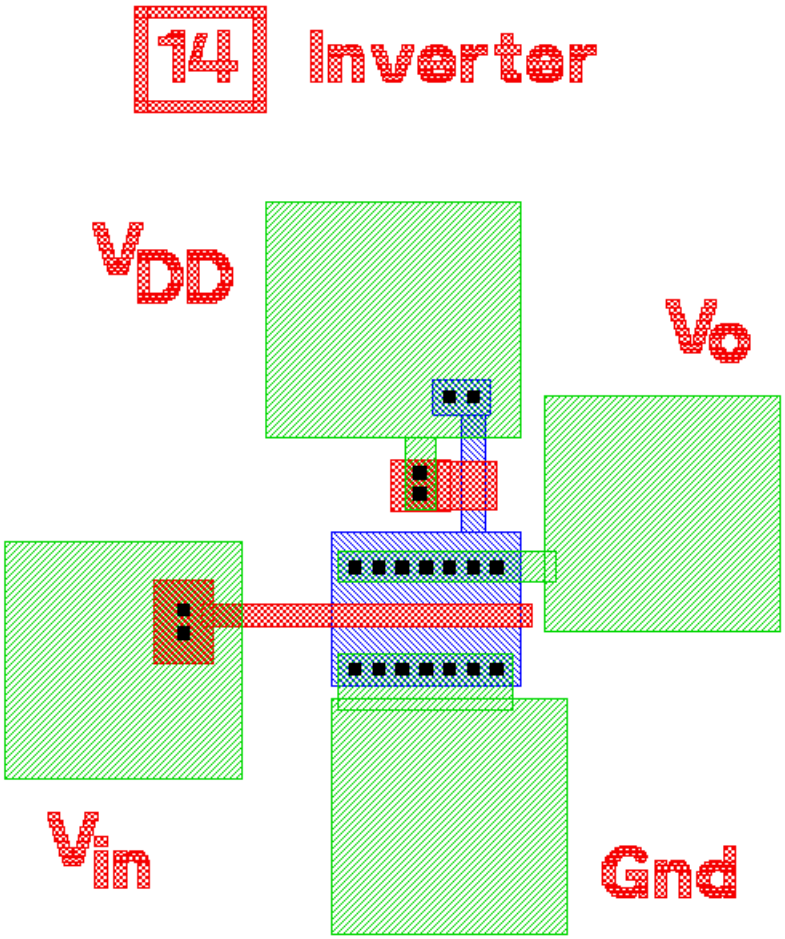



C
13c
BJT
x_B = 9μm
E

Inverter Layout:

14) Inverter:

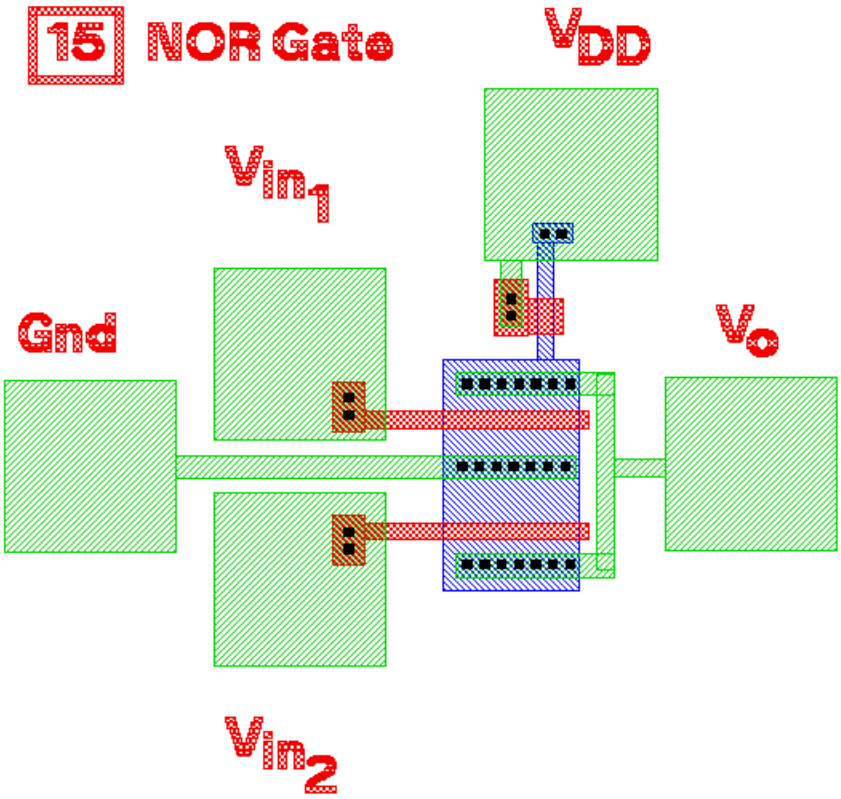
Load: W/L = 10/20 µm
Driver: W/L = 80/10 µm



NOR Gate Layout:

15) NOR Gate:

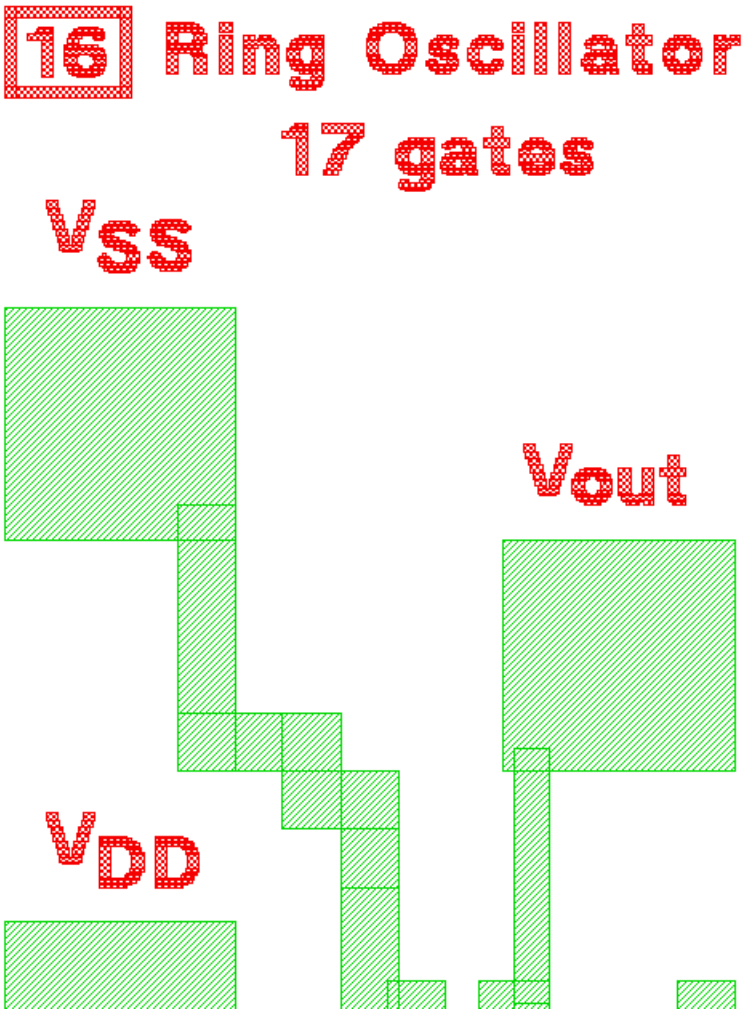
Load: W/L = 10/20 µm
Driver: W/L = 80/10 µm

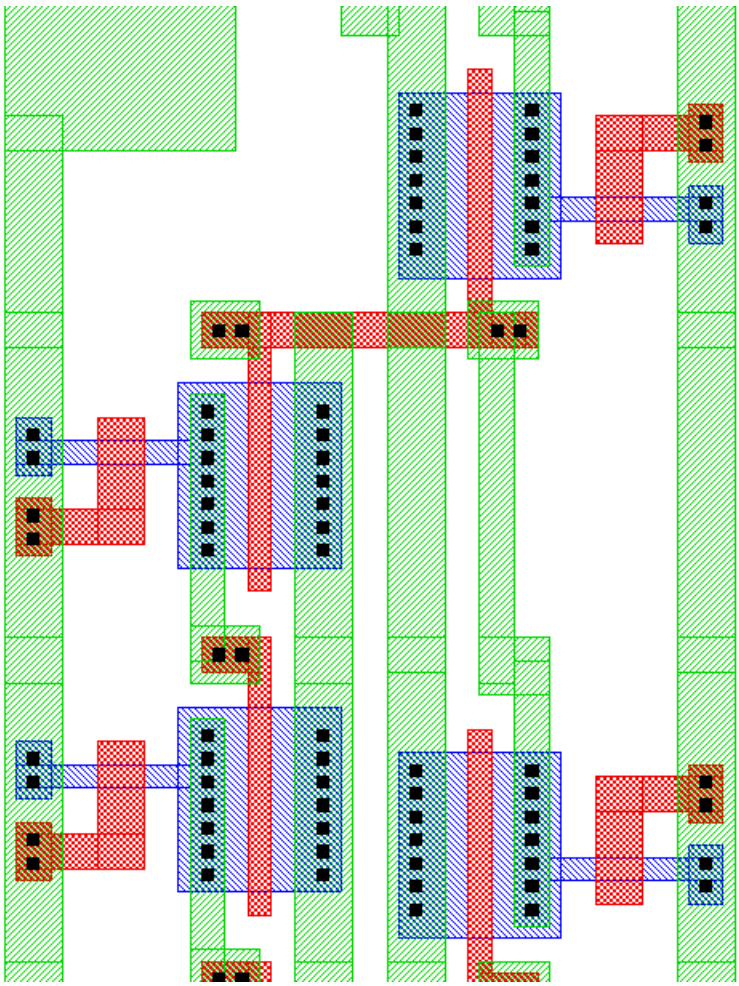


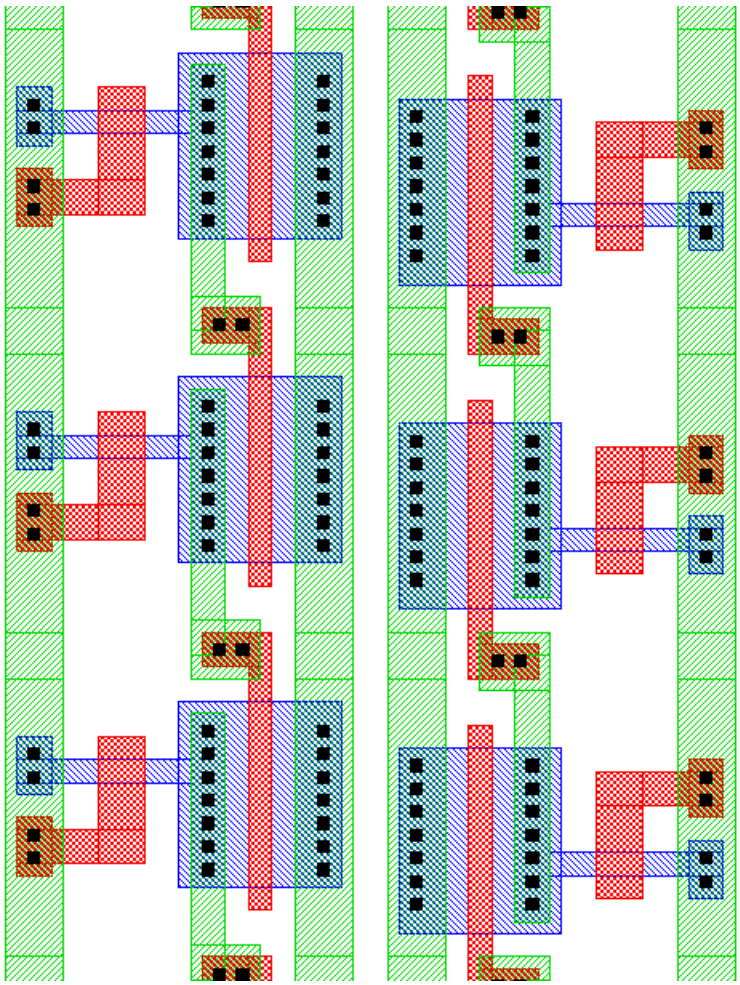
Ring Oscillator Layout:

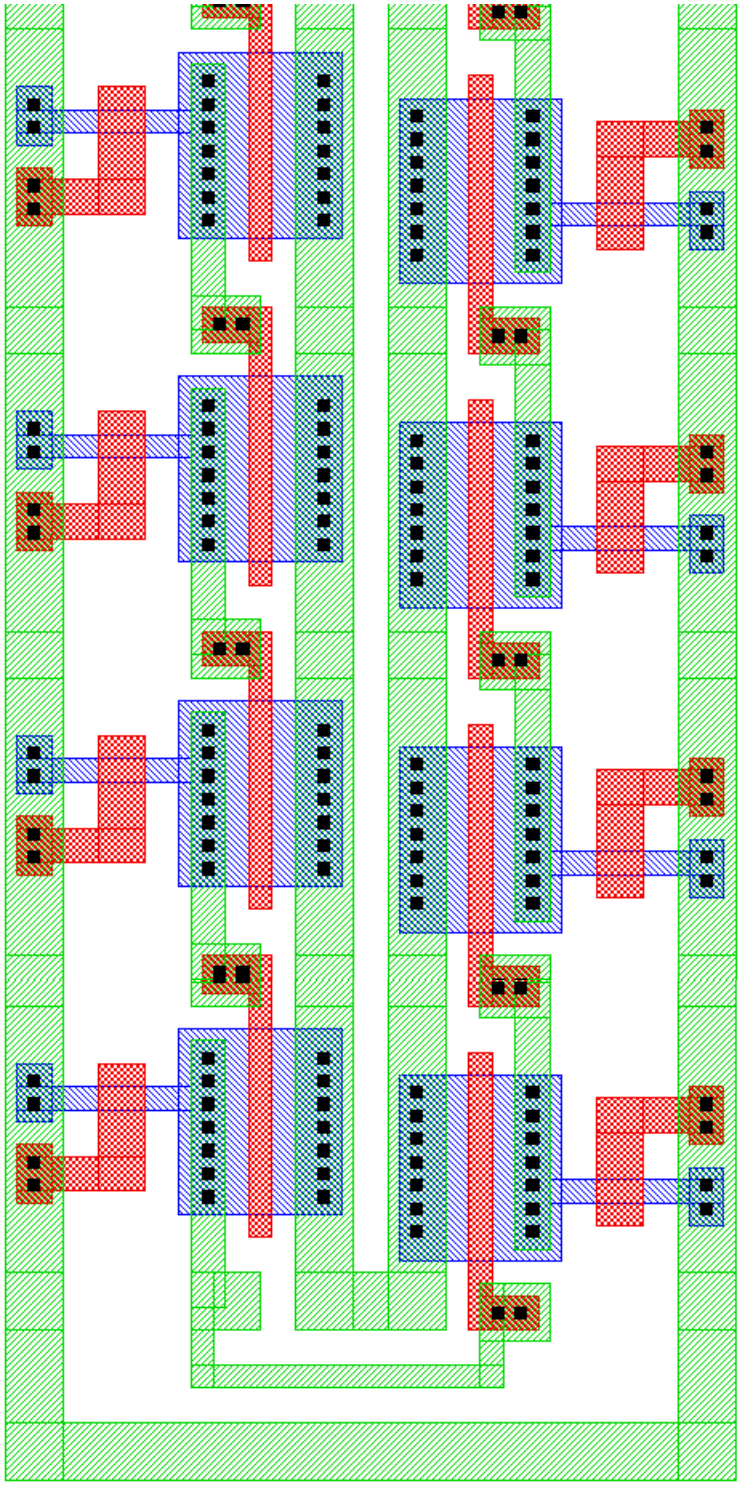
16) Ring Oscillator (17 stages + buffer):

Load: W/L = 10/20 µm
Driver: W/L = 80/10 µm









Layout Designers

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