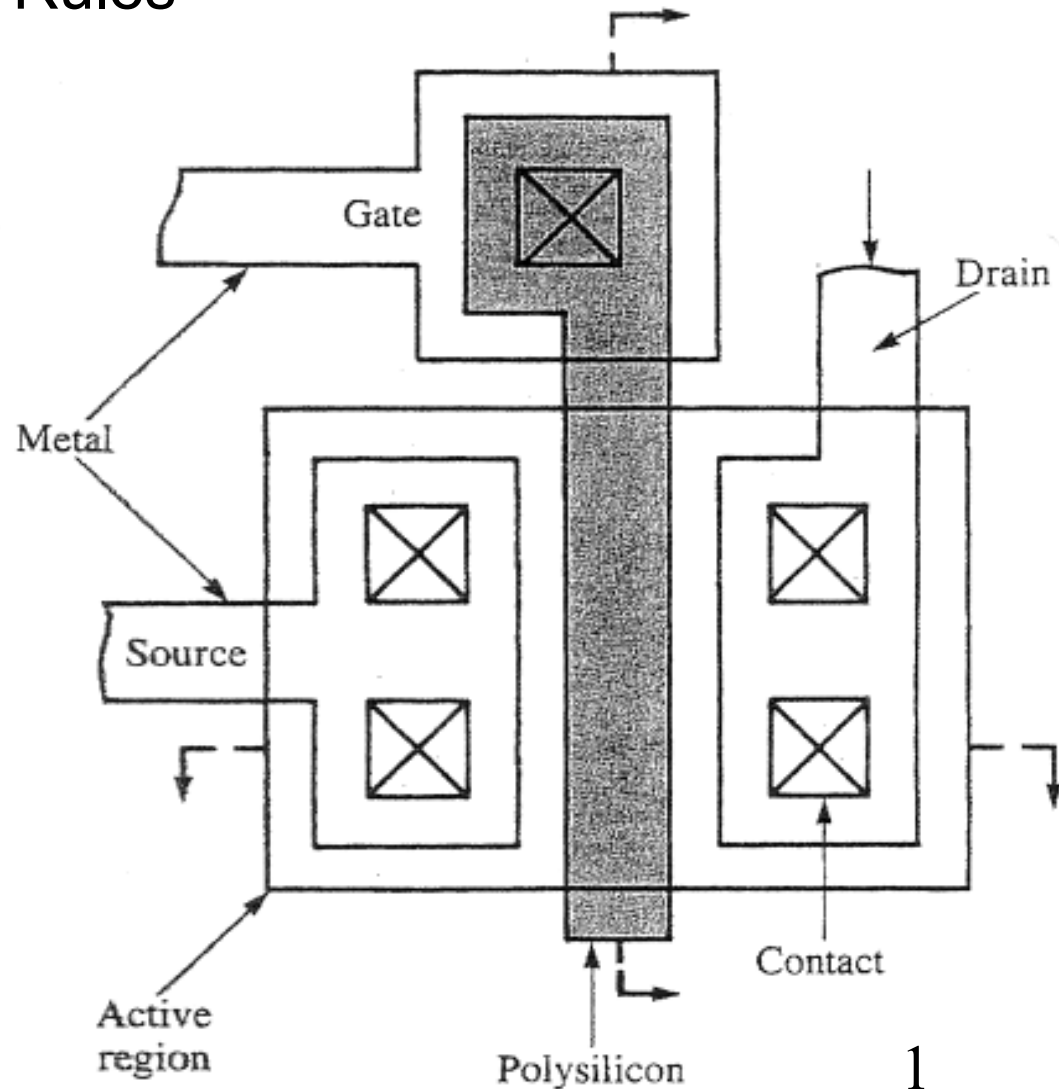


# Layout Design Rules

## (1) Absolute-Value Design Rules

\* Use absolute distances

## (2) $\lambda$ -based Design Rules

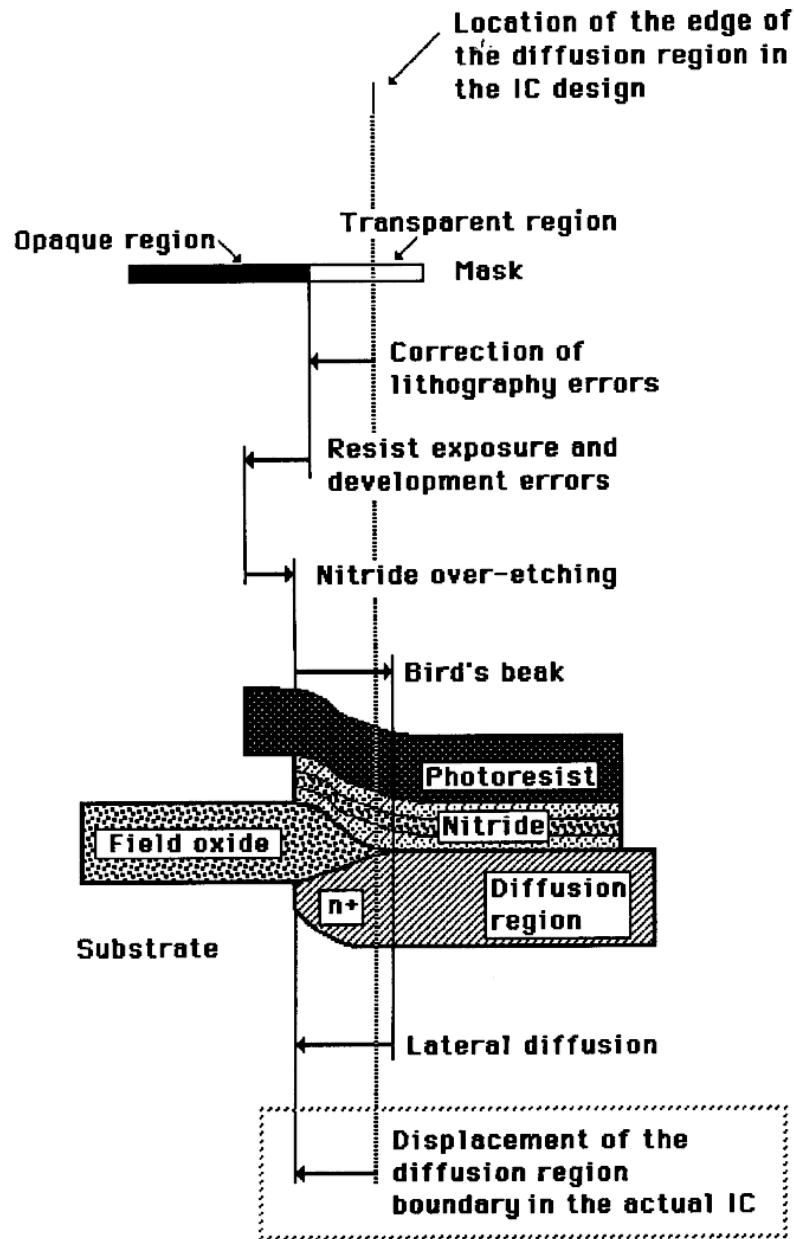


# EE143 Layout Design Rules

1. Basic length unit =  $\lambda = 2\mu\text{m}$

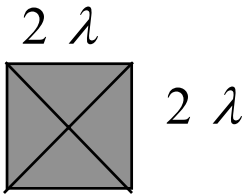
1.1 Lithography and etching limit =  $2\lambda$

1.2 Overlay accuracy =  $\lambda$



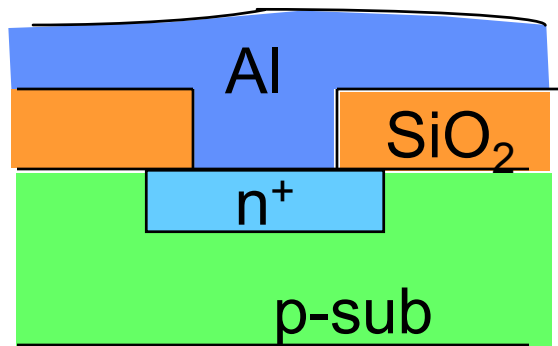
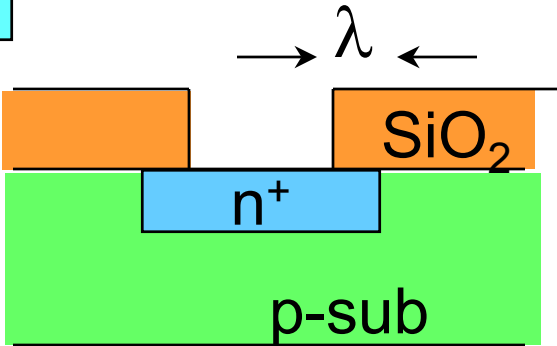
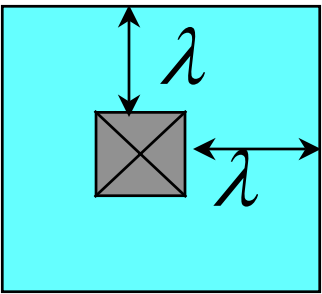
# 2.1 Metal-Si Contact Hole

(same rule for Metal-poly)



Min. contact hole =  $2\lambda \times 2\lambda$

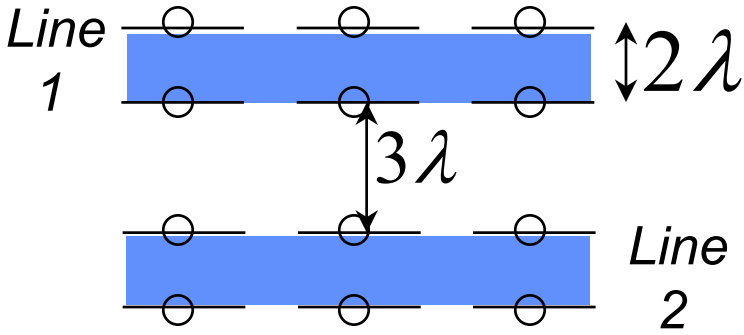
Min contact hole to diffusion layer distance =  $\lambda$



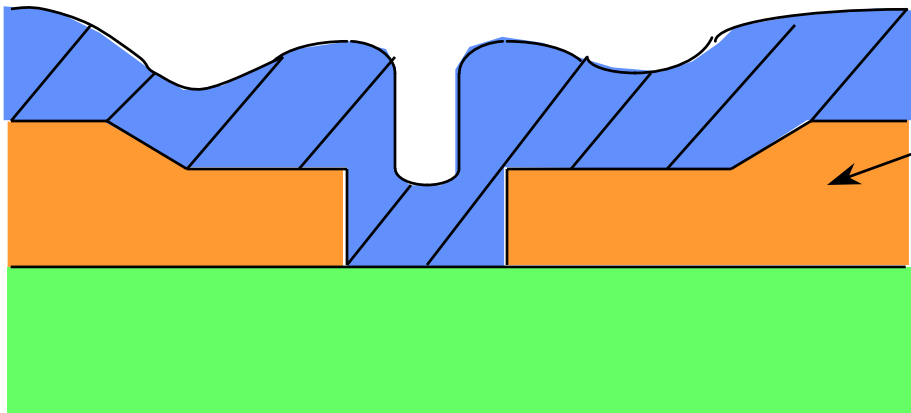
# 2.2. Metal Lines

Min width =  $2\lambda$

Min. metal-metal spacing =  $3\lambda$



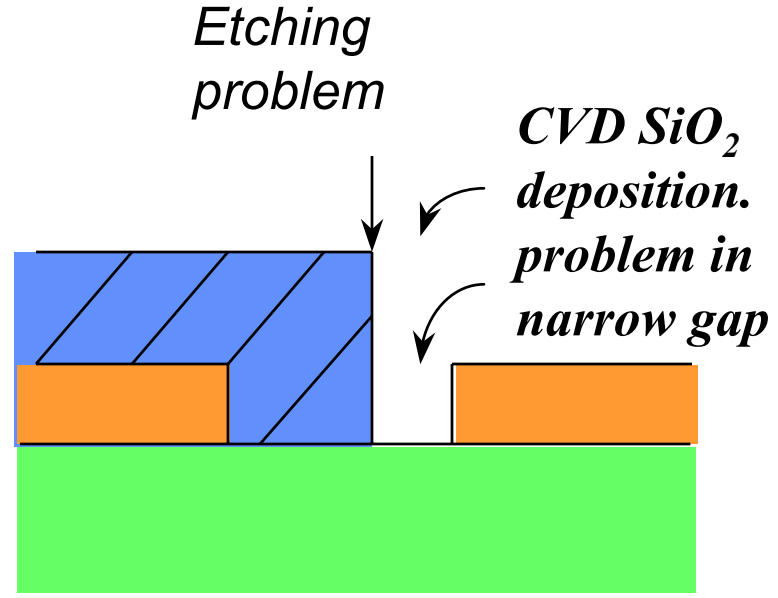
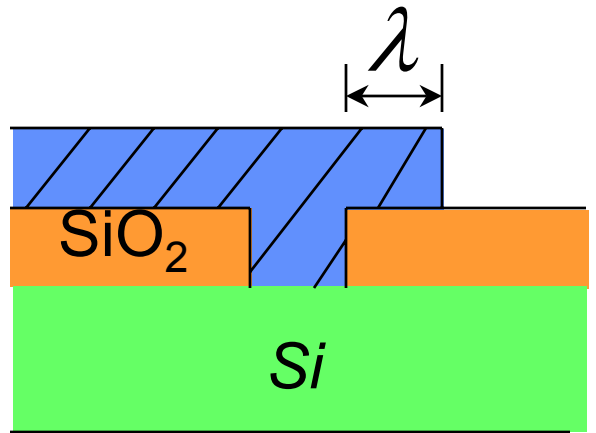
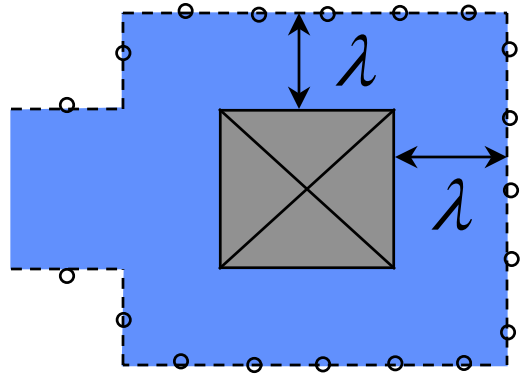
[Rationale]



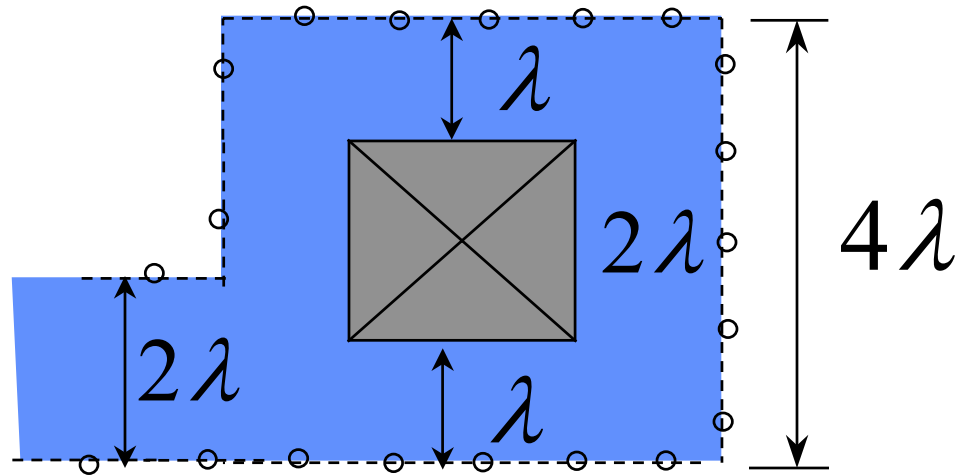
*metal runs on rough topography*

$3\lambda$  spacing to ensure no shorting between the 2 lines.

# Min overlap of contact hole = $\lambda$

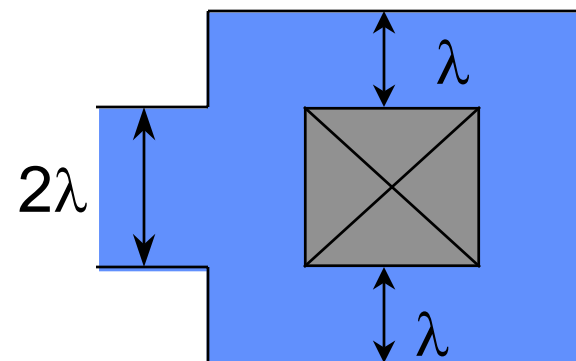


Metal line-width is larger when running over a contact hole



Configuration 1

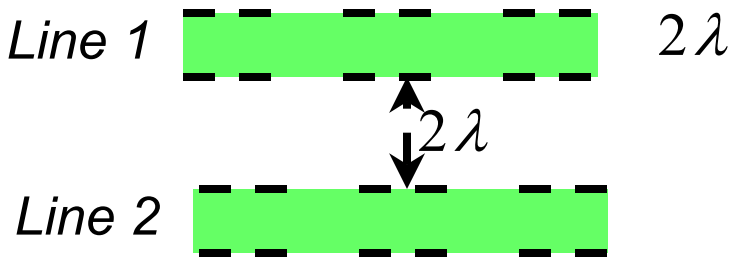
Configuration 2



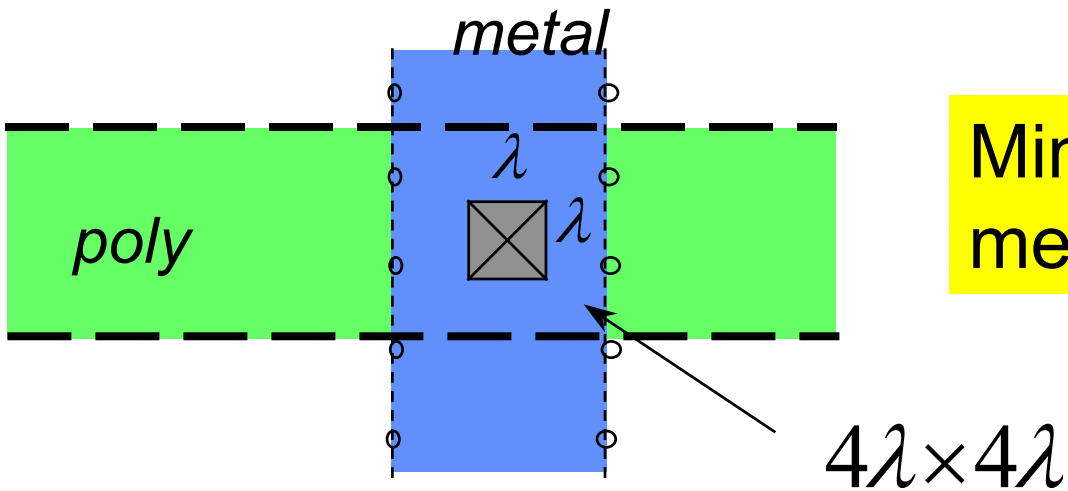
# 2.3 Poly-Si Lines

Min width =  $2\lambda$

Min poly-poly spacing =  $2\lambda$

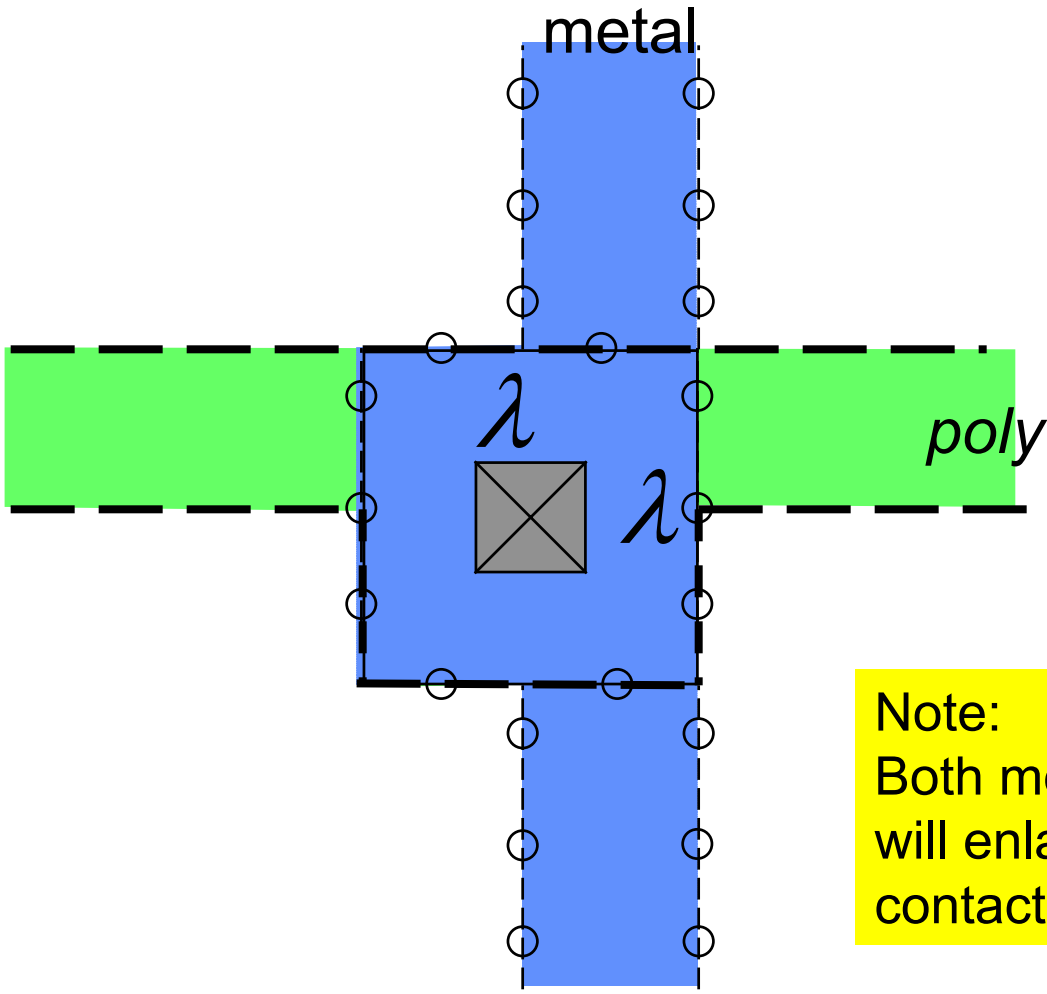


*[Rationale: Unlike metal lines, poly-Si runs on smoother topography]*



Min underlap of metal/poly contact =  $\lambda$

# Example: Metal Contact to Poly

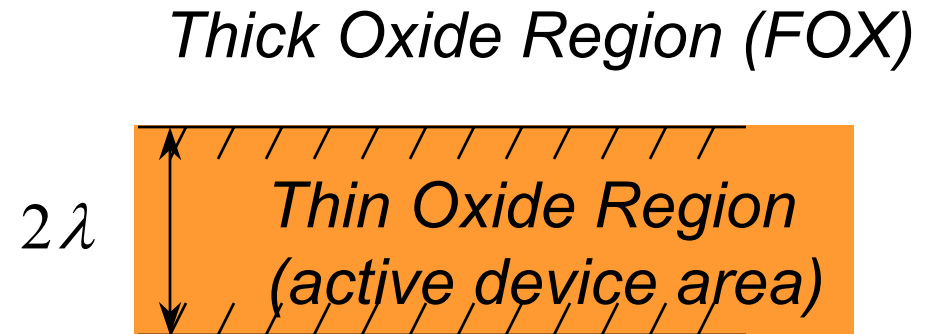


Note:  
Both metal and poly linewidths will enlarge to accommodate contact hole overlay error  $\lambda$

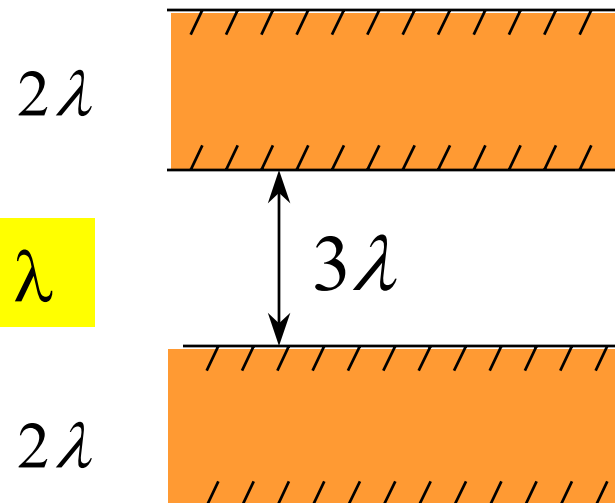


## 2.4. MOS Thin-Oxide Region

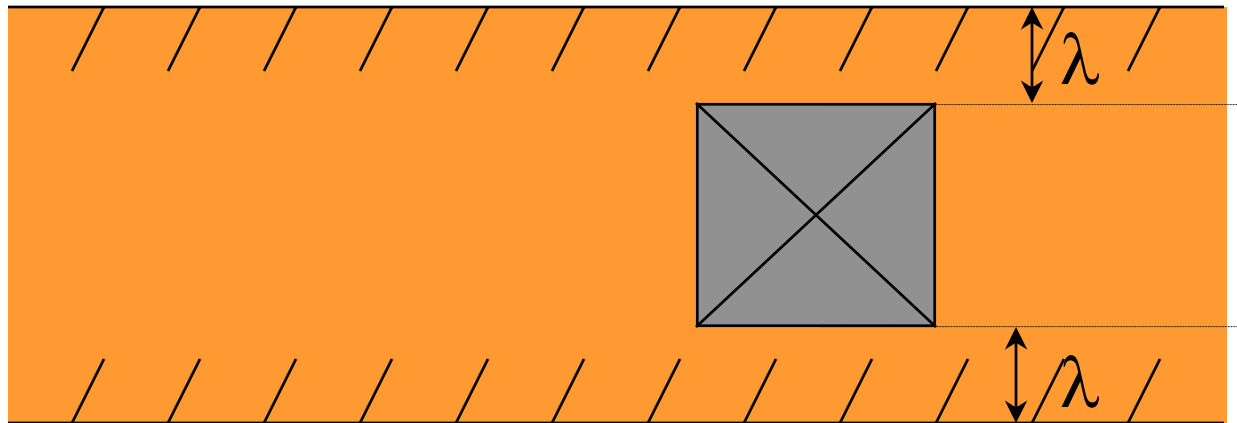
Min Width =  $2\lambda$



Min spacing =  $3\lambda$

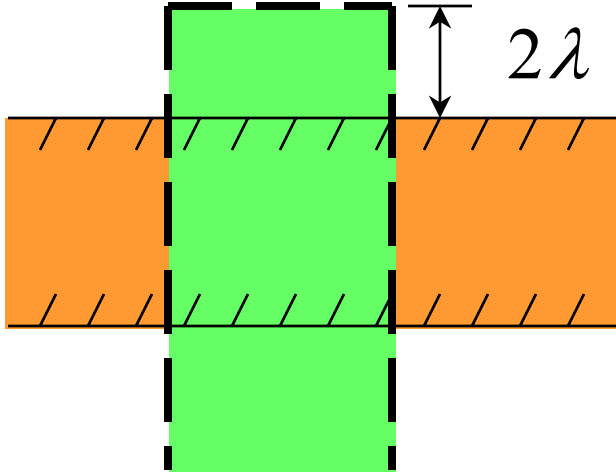


Min underlap of thin-oxide contact =  $\lambda$

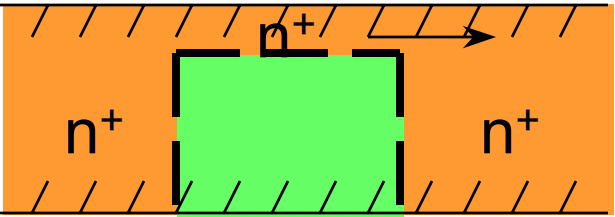
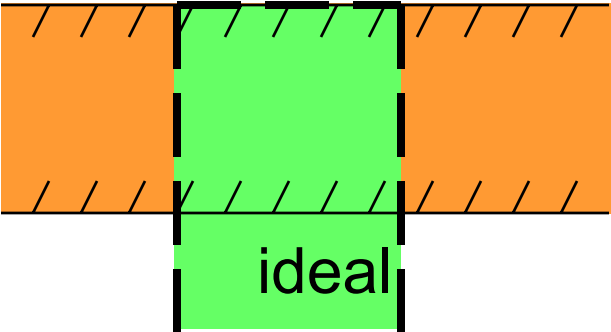


# 3. Poly-Si Gate

Min gate-overlap of field oxide =  $2\lambda$

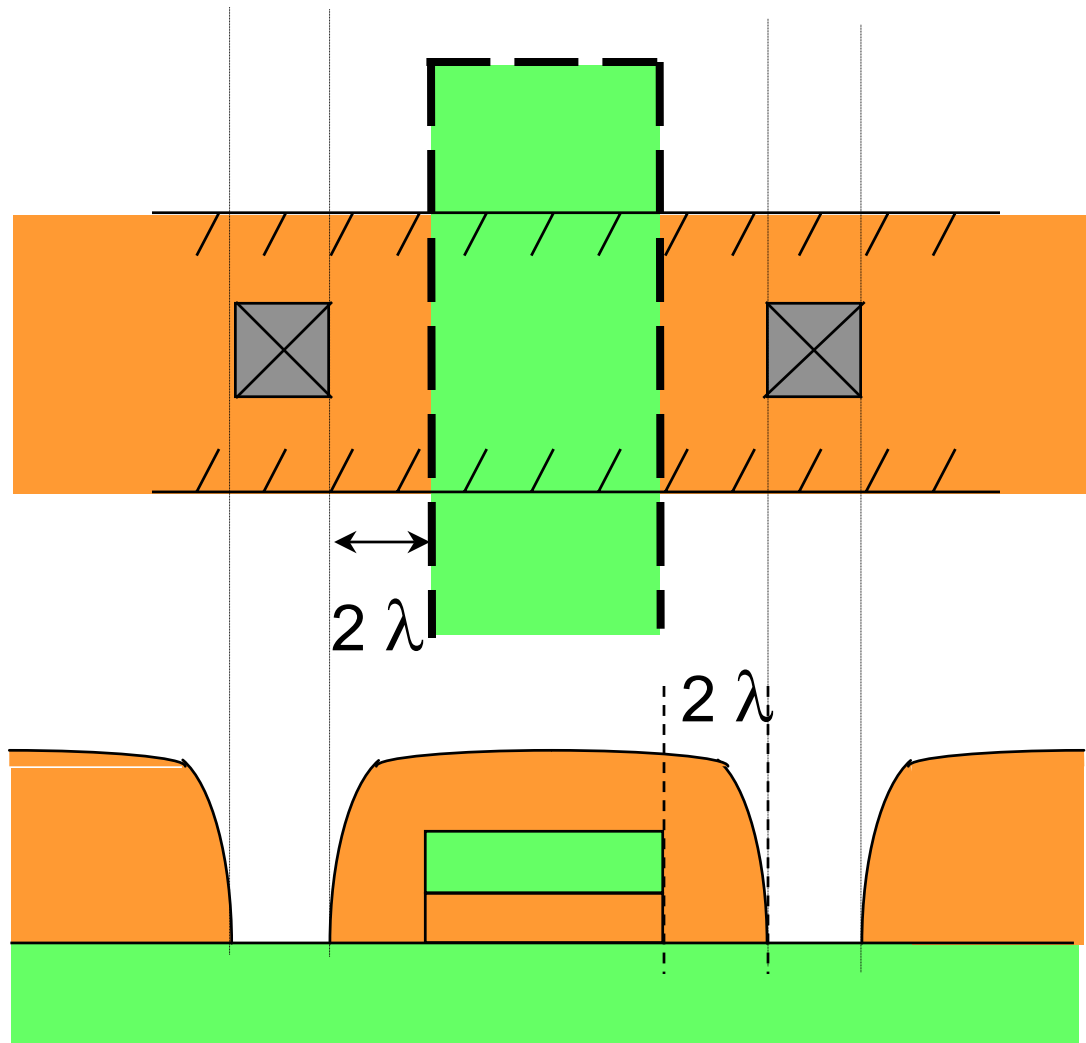


[Comment] Avoid n+ channel formation during S/D Implant

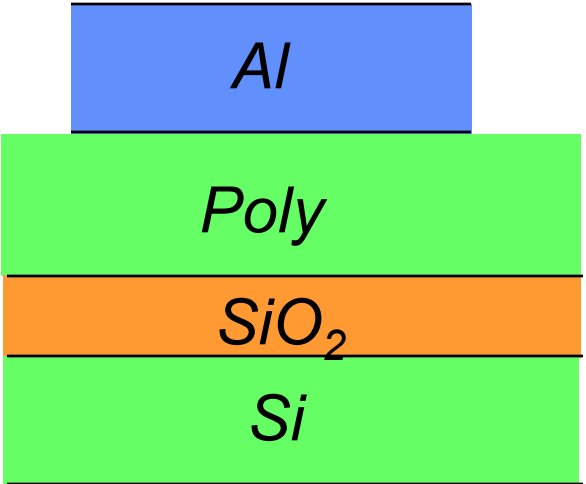
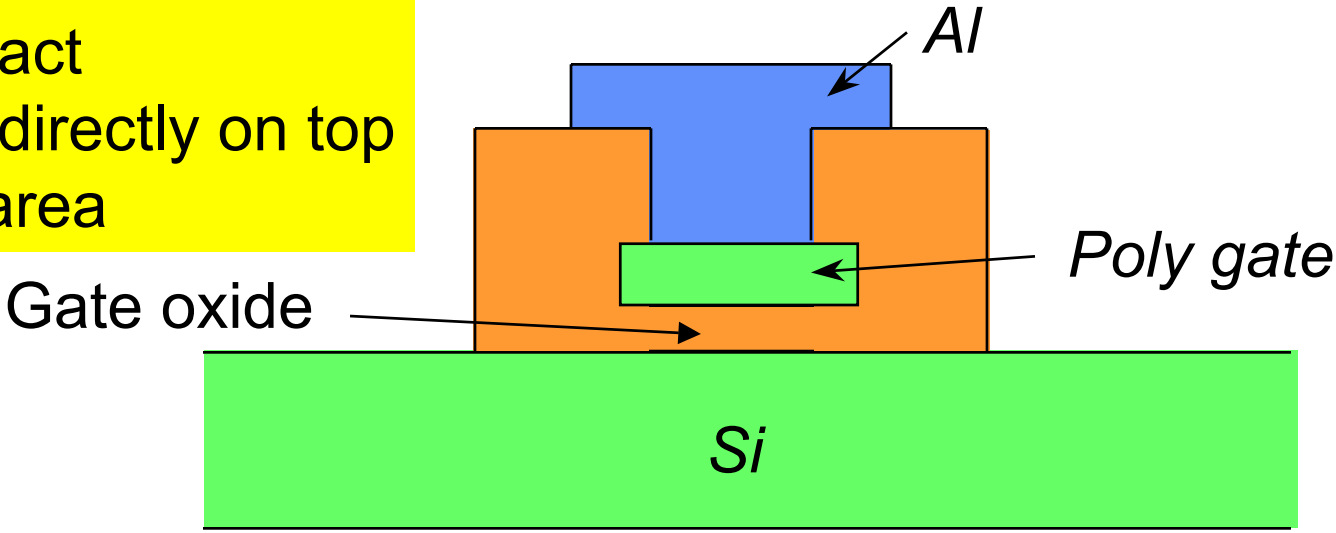


With overlay error

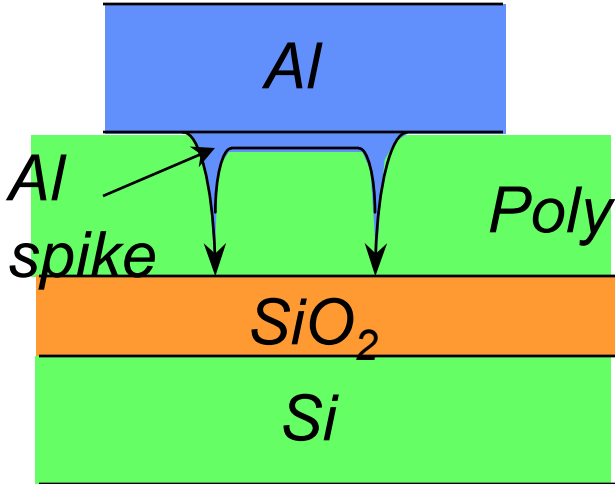
Min thin-oxide contact to gate spacing =  $2 \lambda$

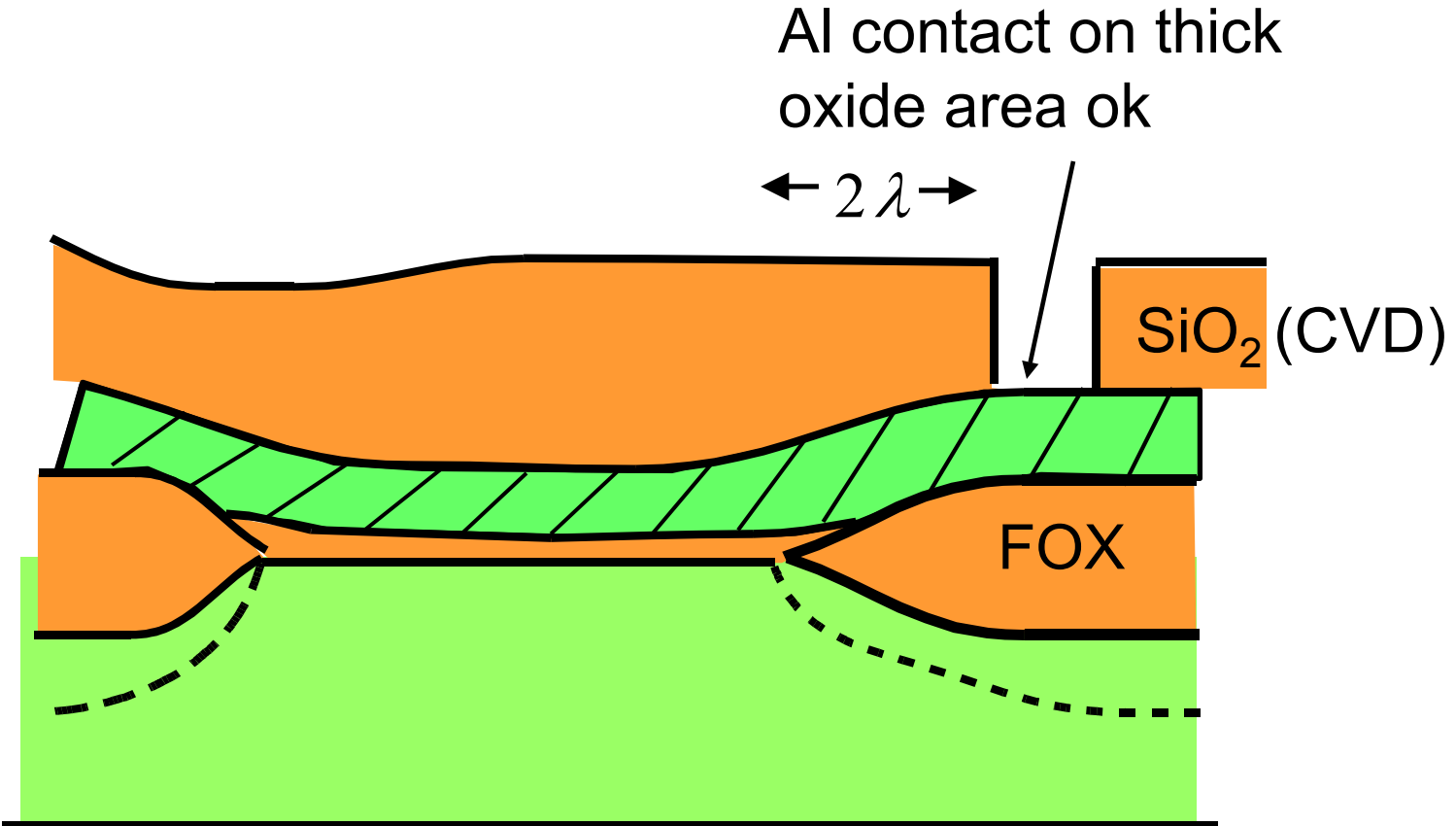


Comment:  
 Al to poly contact  
 should not be directly on top  
 of gate oxide area



~400°C  
 →



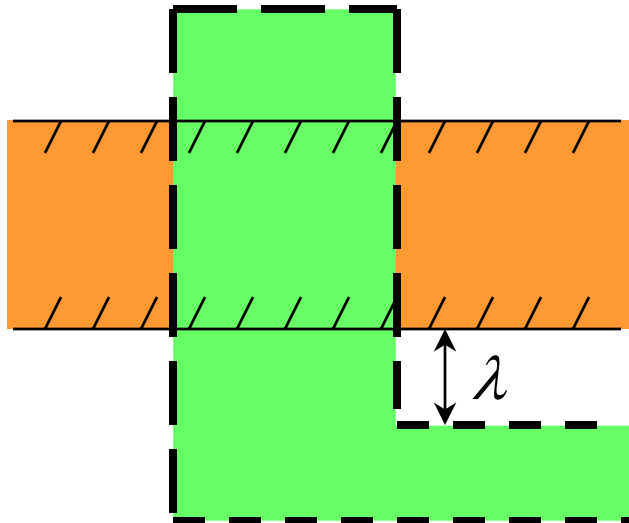


Min Gate Width =  $2\lambda$

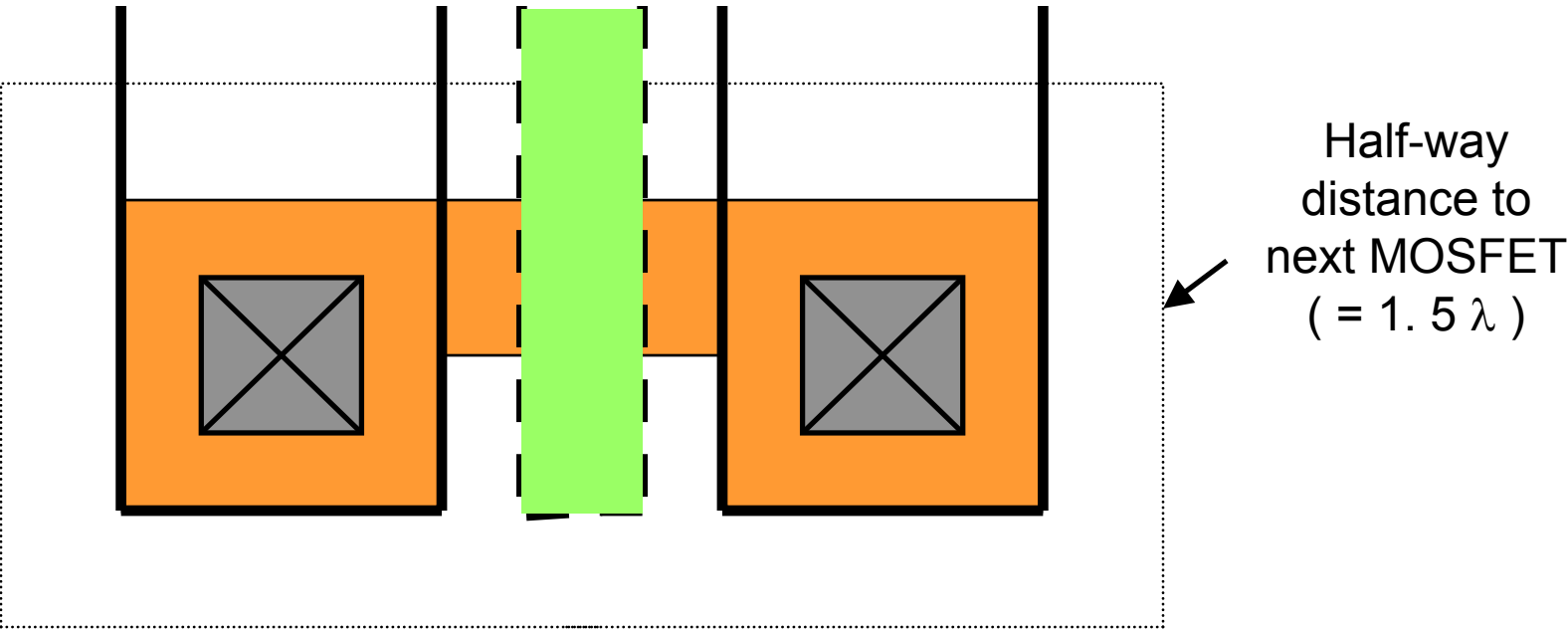
Min Gate Length =  $2\lambda$

Usually: W/L are specified by circuit requirement.





Min. poly to thin oxide spacing =  $\lambda$



Example Design a minimum-size poly-gate MOS transistor with  $W/L = 4\mu\text{m}/4\mu\text{m}$  ( $2\lambda \times 2\lambda$ )



- Minimum size contact =  $2\lambda \times 2\lambda$
- Minimum thin-oxide-region underlap of contact =  $\lambda$
- Minimum source/drain contact to gate spacing =  $2\lambda$
- Minimum L =  $2\lambda$  Minimum W =  $2\lambda$
- Minimum gate overlap of field-oxide region =  $2\lambda$
- Minimum metal overlap of contact =  $\lambda$
- Minimum thin-oxide-region to thin-oxide-region spacing =  $3\lambda$
- \* Layout area /transistor =  $15\lambda \times 7\lambda = 105\lambda^2$

-  metal
-  poly
-  Active region
-  Contact hole