Experiment 6
Gated Lateral BJT Characteristics

W.T. Yeung, W.Y. Leung, S. Pimputkar,
J.W.P. Chen, W. Belachew, and R.T. Howe

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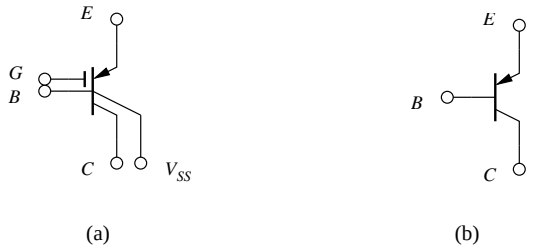
Contents

1 Objective

In this lab, you will characterize a gated lateral BJT. After a brief introduction to gated lateral BJT's and how they differ from conventional pnp BJT's, you will measure all the parameters needed to model the device using the full Ebers-Moll pnp BJT model, a large-signal model. This will be done both using the HP-4155 and more basic equipment. Next,

FIGURE 1. Circuit Symbol for (a) the gated lateral BJT, and (b) the canonical pnp BJT.



(a) (b)

for each region of operation, you will observe how the BJT operates and derive the corresponding simplified Ebers-Moll circuit model. Optionally, you will use the collected data to write a SPICE model for the BJT and use it run sample simulations. The key concepts introduced in this laboratory are:

- Determination of the Ebers-Moll large signal parameters β, V_A, and I_S
- The four regions of operation of the BJT
- Determination of the region of operation from the voltages V_{EB} and V_{CB}

2 Gated Lateral BJT Usage

In this lab, you will not be using a using a conventional BJT, but rather a gated lateral BJT; you will need to be aware of the differences between the two to do the lab. As you know, the vast majority of modern microchips (including the EE105 lab chip) are manufactured in CMOS processes, which do not accomodate for bipolar transistors. Nevertheless, under certain bias conditions, several second-order effects in the p-MOSFET become dominant and the pnp sandwich formed by source, n-well, and drain acts like a pnp BJT perturbed by nonidealities introduced by the gate and substrate which contact the pnp sandwich. This device is called a *gated lateral BJT* (or more commonly *lateral BJT*, if it is clear one is refering to a CMOS process), and is given the circuit symbol shown in Fig. 1(a); the symbol for a canonical BJT as covered in lecture is shown in Fig. 1(b) for comparison.

2.1 Layout and Cross Section

To better understand the structure, consider the gated lateral BJT layout and cross section, shown in Fig. 2. Most of the structure is needed simply to contact the various regions. At the center of the layout is a p-MOSFET whose gate has been fingered for compactness following common MOSFET layout practice. The four diffusion regions are alternately part of the source and drain (which will now serve as the emitter and collector respectively). Two small strips of layer 1 metal connect to the two source diffusion regions via three contacts apiece; a fork-shaped layer 2 metal wire labeled *E* then connects to both metal 1 strips through a via each. A similar structure is used for the collector, labeled *C*.

As indicated by the circuit symbols in the cross section, the heart of the BJT is the pnp sandwich of MOSFET source diffusion, n-well, and drain diffusion. The n-well serves as the base and is (Ohmically) contacted by the base wire through a ring-like n^+ diffusion

FIGURE 2. Gated Lateral BJT Layout and Cross Section

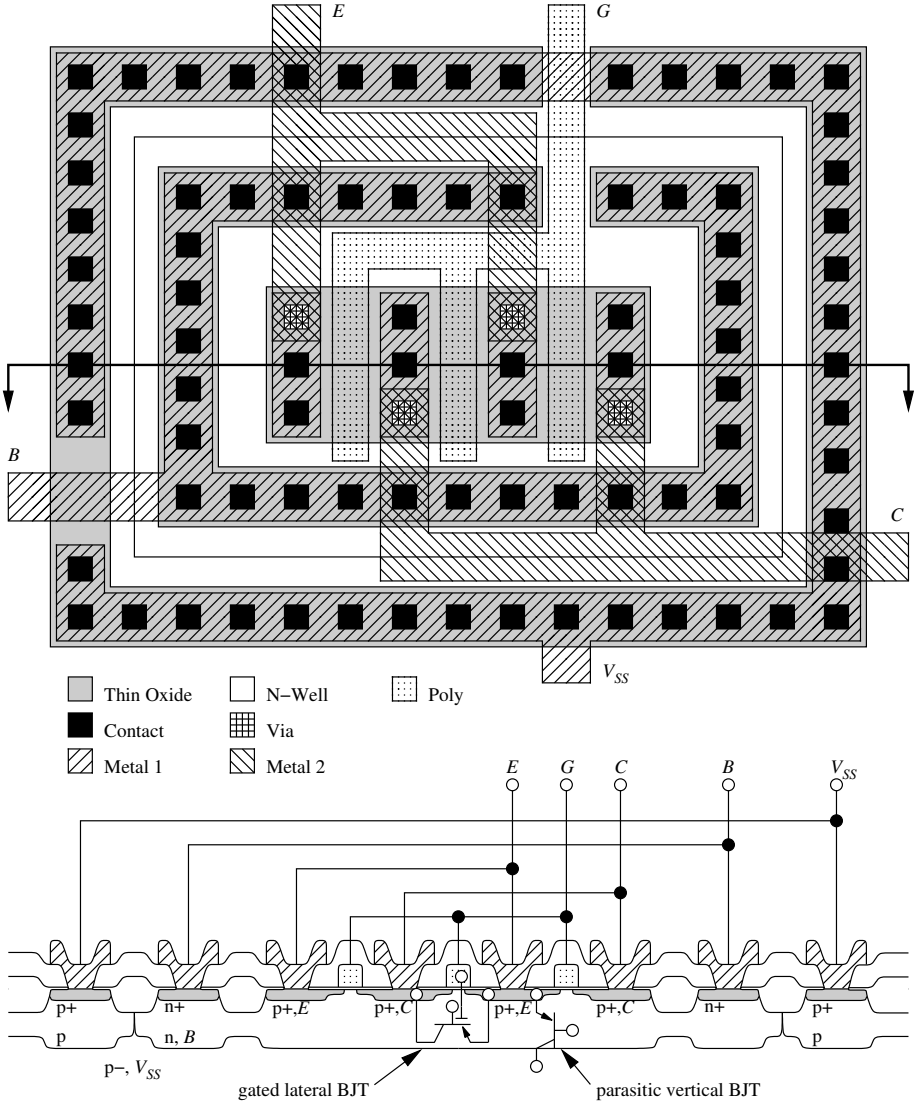


FIGURE 3. MOSFET Cross Section with Indicated Paths for Potential Plots

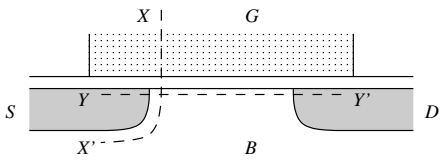
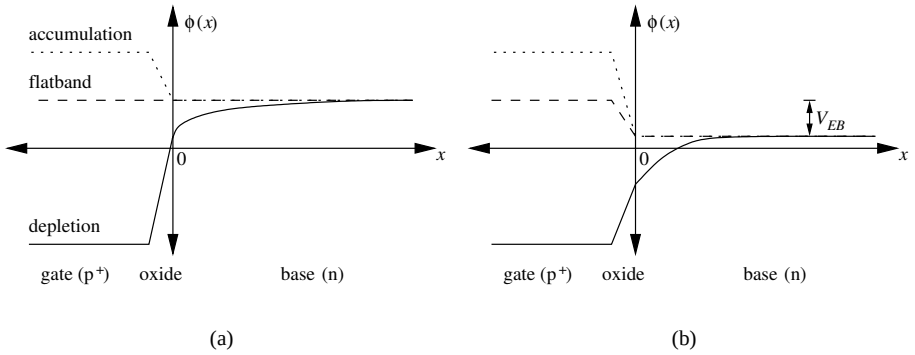


FIGURE 4. Potential Plots along Path XX' in Fig. 3 for (a) zero emitter junction bias, $V_{EB} = 0$, and (b) forward emitter junction bias, $V_{EB} > 0$.



surrounding the MOSFET in the layout. As seen in the cross section, the substrate contacts the n-well as well and represents a second parasitic collector, labelled V_{SS}. It is necessary to draw off the emitter current extracted by the substrate lest it disturb the surrounding circuitry or even trigger latchup (a destructive situtation in which the junctions of parasitic pnpn sandwichs are locked into forward bias). Similar to the n-well/base, the substrate is contacted by a ring-shaped diffusion surrounding the n-well, called a guard ring since it serves to guard against latchup.

2.2 Effect of the Gate: Surface vs. Subsurface Current

The effect of the gate can be completely eliminated by biasing the MOS structue at flatband or in accumulation, $V_{GB} \geq V_{FB}$. This is best understood by considering the potential curves for the MOS structure, shown in Fig. 4(a) for the case $V_{EB} \equiv V_{SB} = 0$ and in Fig. 4(b) for the case $V_{EB} \equiv V_{SB} \geq 0$ At flatband and in accumulation, the potential level is flat throughout the base. If there were no gate at all, this uniform potential would be interpreted as steming from a uniform base doping, which is assumed in the 1-dimensional BJT model covered in lecture. In depletion, the gate bends down the potential curves in the base near the silicon surface, corresponding to reduced base doping at the surface. While this low effective base doping can be used to advantage to produce BJT's with extremely high values of common-emitter current gain β (beyond 10^6), nonuniform base doping is not covered by the 1-dimensional model you covered in lecture, and therefore it will be easier for us to build a BJT with equivalently uniform base doping by biasing $V_{GB} \geq V_{FB}$ and then just ignore the gate completely.

2.3 Effect of the Substrate: Current Splitting

As pointed out in the discussion of the cross section, the substrate forms a parasitic second collector which collects about 30% of the emitter current, an effect called current splitting. Unlike with the gate, this effect cannot be eliminated (at least not with the gate bias we will be using.) Our approach will be to ignore the substrate current I_{SS}, with the following caveats:

- The collector current I_C is now too low by the amount I_{SS} in forward-active region. In reverse-active region, I_C will be at its full value and thus appear higher than expected by the amount I_{SS}.
- Since α is defined as $\alpha \equiv -I_C/I_E$ while $\beta \equiv I_C/I_B$, we now have

$$\alpha = -\frac{I_C}{I_E} = \frac{I_C}{I_C + I_{SS} + I_B} = \frac{I_C/I_B}{I_C/I_B + I_{SS}/I_B + I_B/I_B} = \frac{\beta}{\beta + \beta_{SS} + 1} \neq \frac{\beta}{\beta + 1},$$

  where $\beta_{SS} = I_{SS}/I_B$ denotes the common-emitter current gain of the parasitic collector. However, in order that you will get used to using the correct formula for regular BJT's, you will calculate the common-gate current gain as $\tilde{\alpha} = \beta/(1+\beta)$ except where indicated otherwise.
- Since the emitter current is no longer approximately equal the collector current, you will need to keep I_C well below 1 mA to ensure I_E never reaches 1 mA.
- The common-collector and common-emitter characteristics of the BJT will no longer be identical. Although the common-emitter configuration is much more common in practice, its characteristics for the gated lateral BJT look somewhat different from those of a regular BJT, so common-collector configurations have been adopted in this lab.
- You will not be able to fully model this device using the standard BJT model in SPICE.

2.4 Effect of Doping Levels

As a final note, one needs to be aware that the MOSFET has symmetrically doped source/drain regions, whereas the collector of a conventional BJT is doped much more lightly than the emitter to keep the Early voltage V_A as high as possible. In particular, you will observe almost no difference between forward and reverse active regions (apart from that introduced by any asymmetric sizing of the source/drain diffusions; this is not to be seen in Fig. 2).

3 Prelab

- H & S Chapters 7.1–7.4, 7.7 (skip 7.7.2)
- Write down the complete Ebers-Moll Equations for a pnp BJT.
- Write down the simplified equations appropriate for the forward active and reverse active regions. From these equations, derive the Ebers-Moll large-signal model for both these regions of operation.

TABLE 1. Configuration of **Channels: Channel Definition** and **Measure: Sweep Setup** pages

Unit	VName	IName	Mode	Fctn	Value	Compliance
SMU1:MP	***VC***	***IC***	***V***	***CONST***	0 V	1 mA
SMU2:MP	***VB***	***IB***	***I***	***VAR2***	$-\{20, 40, \ldots, 80\}\,\mu$A	2.5 V
SMU3:MP	***VE***	***IE***	***V***	***VAR1***	$[0, 2]$ V	1 mA
SMU4:MP	***VSS***	***ISS***	***V***	***CONST***	0 V	1 mA
VSU1 (or VS1)	***VG***	—	V	***CONST***	2.5 V	—

TABLE 2. Pin Assignment for BJT1 on the UCBJ32BJT

Terminal:	C	B	E	V_{SS}	G
Pin Number:	8	7	6	9	5

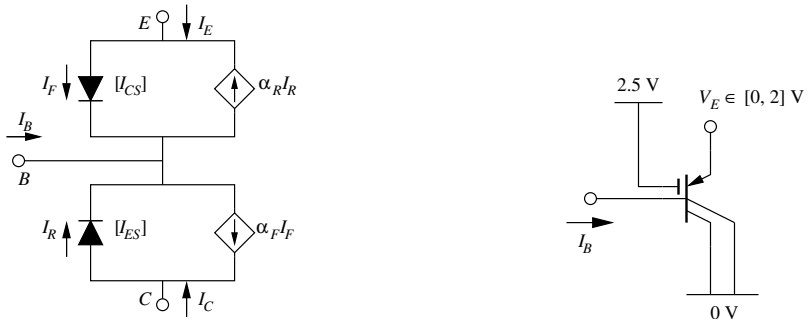
4 Ebers-Moll Model Parameter Extraction

CAUTION: Unlike the Micro Linear chips you have been using so far, this lab's chip (EE105 prototype lab chip UCBJ32BJT) has not yet been equipped with any kind of protection against excessive voltage or current. The chip is therefore extremely delicate, and from experience you *must* take the following three precautions in order to make it through the lab without destroying your chip:

1. To prevent electrostatic discharge:
   - **(a)** Do not touch the pins or any connecting wires. Rather, set up the entire circuit before inserting the chip.
   - **(b)** Always ground yourself before handling the chip, especially if for some reason you are forced to touch a pin. (You can ground yourself by touching the bare metal chassis of any piece of equipment which is equipped with a three-pronged plug and is plugged into a wall socket.)
2. Do not exceed the voltage and current compliance values of 2.5 V and 1 mA respectively. (These allow for a mere 20 % safety margin before the chip will break.)
3. Finally, read and follow directions carefully: skimming the directions will likely lead you to overbias the chip in some nonobvious way.

Shown in Fig. 5(a) is the complete Ebers-Moll model for the pnp bipolar junction transistor. You will find all the parameters for this model in this experiment: β_F, β_R, V_{AF}, V_{AR}, (I_{ES}, I_{CS},) and I_S.

FIGURE 5. (a) Ebers-Moll Model for the pnp BJT. (b) HP-4155 Configuration.



(a) (b)

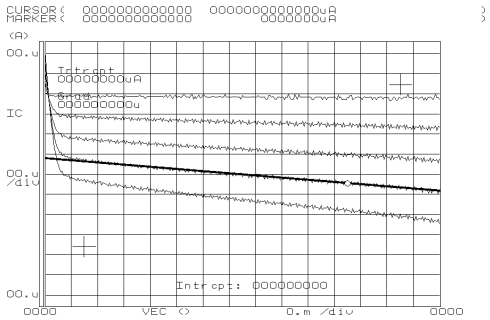
4.1 Parameter Extraction Using the HP-4155

4.1.1 Extraction of β_F, β_R, V_{AF}, V_{AR}

In this section, you will use the HP-4155 to do an I_C–V_{EC} plot and determine the forward-active region parameters β_F and V_{AF}. Doing a similar I_E–V_{CE} plot will then yield the reverse-active region parameters β_R and V_{AR}.

1. Configure the **Channels: Channel Definition** page as shown in Table 1 and illustrated in Fig. 5(b). (Note VSU stands for Voltage Source Unit [1]; on the HP-4145B this is abbreviated VS instead.)
2. On the **Channels: User Function Definition** page, define ***VEC*** with units of ***V*** as ***VE-VC***.
3. Configure the **Measure: Sweep Setup** page as shown in Table 1. The I_B values have been chosen to prevent I_E (and hence all other terminal currents) from reaching compliance.
4. Configure the **Display: Display Setup** page to display a linear-linear I_C–V_{EC} plot over the range $0\,\text{V} \le V_{EC} \le 2\,\text{V}$ and $-0.2\,\text{mA} \le I_C \le 1\,\text{mA}$.
5. Observing the precautions given on page 6, place the UCBJ32BJT into the test fixture and connect it with the SMU's and VSU (or VS). For the pin assignment see Table 2.
6. Run the test program and note the curves traced out by the HP-4155.
7. Find β_F by comparing the collector current with its corresponding base current.
8. Find the Early voltage V_{AF} by fitting a line to one of the I_C-V_{EC} curves. (If your data are noisy or contain oscillations, or if you want a more accurate measurement, and you are using an HP-4155ABC, you will want to use the analyzer's regression line analysis function to do this, described in Fig. 6.) Note that these values of V_{EC} are low enough that you will not observe punchthrough effects, which cause I_C to blow up as the punchthrough voltage $V_{EC} \approx 5\,\text{V}$ is approached.

FIGURE 6. Using Regression Line Analysis on the HP-4155ABC to Find V_A



The procedure to find the regression line [1] is similar to the two-point line fitting method from previous labs:

1. On the **Graph/List: Graphics** page, select the {**Marker/Cursor**} primary softkey if necessary, then set the {**Marker**} secondary softkey to {**On**}.
2. If multiple graphs are plotted, first select the proper axis using the {**Axis**} primary softkey, then skip to the desired measurement curve using the {**Marker Skip**} secondary softkey. (If all curves intersect under the marker, you may need move it using the knob.)
3. Select the {**Line**} primary softkey. Set the {**Line Select**} secondary softkey to {**1**} or {**2**}. Toggle on the {**Line**} secondary softkey. Toggle on the {**Regress Mode**} secondary softkey.
4. The part of the curve that falls inside the rectangle having the two cursors as its opposite endpoints is used to find the regression line. (See screenshot above.) Move the cursors using the arrow keys (holding **[Fast]** if desired) and select the cursor to move via the {**Select Cursor**} secondary softkey.

9. Get a hardcopy of the I_C–V_{EC} curve. You can print PCL files in 353 Cory by opening a Windows command prompt and typing

   ```
   lpr -S korchnoi -P print353 -o l filename.pcl
   ```

   (The `-o` argument is the lowercase letter L.)

10. Interchange the connection for the collector and emitter and repeat steps 6 to 9 to find β_R and V_{AR}. Compare the forward- and reverse-active region curves by
    - **(a)** explaining what differences you would expect for a conventional BJT, and
    - **(b)** explaining what you actually observe for this gated lateral BJT (see Secs. 2.3 and 2.4).

4.1.2 Extraction of I_S

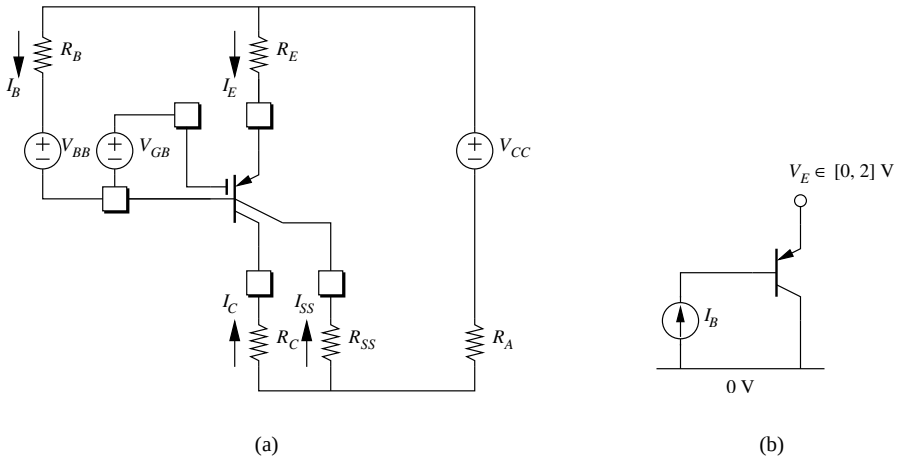
In this section you will calculate I_S from I_{ES} and I_{CS}, which you will in turn obtain by plotting I_E vs. V_{EB} and I_C vs. V_{CB} respectively. This will complete the extraction of all Ebers-Moll model parameters via the HP-4155.

1. Press button **[Chan]** to go back to the **Channels: Channel Definition** page and load the program {**(Mem4) Diode VF–IF**}. You will get the setup shown in Table 3. Here, I_F and V_F will represent I_C and V_{EB} respectively.
2. Connect SMU 1 to the emitter and SMU 3 to the base. Short the collector and substrate to the base.

TABLE 3. HP-4155 Diode Characterization Program

Unit	VName	IName	Mode	Fctn
SMU1:MP	VF	IF	V	VAR1
SMU2:MP				
SMU3:MP	V	I	COMMON	CONST
SMU4:MP				

FIGURE 7. (a) Gated Lateral BJT Test Circuit. (Boxes represent pins, see Table 2 for numbers.) (b) Common-Collector Circuit for SPICE Simulation.



3. Reduce the current compliance from 40 mA to 1 mA.
4. Reconfigure the display to plot, on a log scale, $I_F \in [1\,\text{fA}, 1\,\text{mA}]$.
5. Run the measurement and explain the measured I_E–V_{EB} curve using your knowledge of p^+n junctions. (For example, at high V_F, the low-level injection assumption is no longer valid, causing the slope to eventually fall off to half its ideal value.)

   Evaluate the ideal diode equation at an appropriate point on the curve to find I_{ES}. Then determine I_{ES} automatically by fitting a line to the straight, steep-slope part of the curve. (Use the regression line analysis function if you deem it necessary.) Finally, get a hardcopy of the plot.
6. Connect SMU 1 to the collector instead and repeat step 5 to plot I_C–V_{CB} to determine I_{CS}.
7. Using the values for β_F and β_R you extracted in Sec. 4.1.1, compute $\tilde{\alpha}_F = \beta_F/(1+\beta_F)$ and $\tilde{\alpha}_R = \beta_R/(1+\beta_R)$. Finally, use these two values to compute the transistor saturation current I_S both as $I_S = \tilde{\alpha}_F I_{ES}$ and as $I_S = \tilde{\alpha}_R I_{CS}$.

4.2 Parameter Extraction and Regions of Operation Using Circuit Measurements

In this section you will practice how to extract the Ebers-Moll model parameters if you don't have access to a semiconductor parameter analyzer. In addition, you will see how the

TABLE 4. Measurements for each Region of Operation

Configuration	1	2	3[a]	4
V_{CC}	2 V	1 V	2 V	
V_{BB}	(ramp up for I_C)	−1 V	4 V	4 V
V_{EB}				
V_{CB}				
Region of Operation				
I_C	−0.3 mA			
I_B				
β [b]				
$\tilde{\alpha}$ [b,c]				
I_{ES} or I_{CS} [b]				

[a] Swap emitter and collector for this column.
[b] Enter N/A if not applicable.
[c] Use the formula $\tilde{\alpha} = \beta/(1+\beta)$. The correct value is actually much lower due to current splitting.

BJT works in each of the four regions of operation.

1. Set up the circuit shown in Fig. 7(a), but *do not insert the chip until instructed to do so*. Use $R_C = R_E = R_{SS} = 100\,\Omega$, $R_B = 91\,\text{k}\Omega$, and $R_A = 0$ for now.

   The setup of the power supplies is slightly involved since we need to use the two HP-6235A voltage supplies at each station to produce three bias voltages (represented by voltage sources in Fig. 7(a)). Use the first power supply to implement the voltage source V_{CC}, using the $+6\,\text{V}$ and *Com* jacks for the $+$ and $-$ terminals of the voltage source respectively. Use the second power supply to implement both of the voltage sources V_{GB} and V_{BB} as follows: use the $+6\,\text{V}$, $+18\,\text{V}$, and *Com* jacks respectively for the $+$ terminal of V_{BB}, the $+$ terminal of V_{GB}, and the $-$ terminal common to both voltage sources.

   Set all six jack voltages to zero by rotating all knobs fully counterclockwise. Turn the $+18\,\text{V}$ knob on the second supply to bias $V_{GB} = 1\,\text{V}$ as closely as you can; use a voltmeter to monitor this voltage, waiting about five seconds for the voltage to settle. (This bias achieves $V_{GB} \geq V_{FB} \approx 0.5\,\text{V}$, the motivation for which was given in Sec. 2.2; this value will also be needed for an unrelated reason below.) Be careful not to adjust this knob anymore after this point as the $+18\,\text{V}$ output is applied directly to the device without being divided down first.

2. Observing the precautions given on page 6, you may now go ahead and insert the chip into the circuit.

Lab Tip

Remember that while voltages are measured in parallel, currents must be measured in series. It is often more convenient – and sometimes more accurate – to measure the current via Ohm's Law by measuring the voltage drop across a resistor through which the current flows. If you choose to use the nominal resistance values, note the tolerances of the resistors to know the uncertainty in the measurement.

3. Table 4 lists four bias configurations corresponding to the four regions of operation. For each of columns 1, 2, and 3 of the table, fill in the missing values and sketch the simplified Ebers-Moll circuit model. Use the formula $\tilde{\alpha} = \beta/(1+\beta)$ for the common-base current gain and put N/A where there parameters β,α,I_{ES}, or I_{CS} do not apply. (Leave column 4 blank for now.) Further directions for individual columns follow:

Column 1 Slowly ramp up V_{BB} to the proper value needed to obtain $I_C = -0.3\,\text{mA}$; since I_C is a strong function of V_{EB}, take care not to overbias V_{BB}.

Column 2 Since V_{BB} shares the *Com* terminal with V_{GB}, you cannot simply swap the V_{BB} terminals to obtain a negative V_{BB}; instead you will need to move the plug from the $+6\,\text{V}$ jack to the $-18\,\text{V}$ jack and set that output as follows: The *Track* knob specifies what fraction $\in [0, 1.05]$ of the voltage on the $+18\,\text{V}$ terminal is negated and supplied on the $-18\,\text{V}$ terminal. Since you set the $+18\,\text{V}$ terminal to $1\,\text{V}$, rotate the *Track* knob all the way clockwise to obtain just over $-1\,\text{V}$ on the $-18\,\text{V}$ output.

Column 3 For this step only, swap the emitter and collector. As you will see, this causes the collector to inject rather than collect current. Since the collector will no longer be competing with the substrate for a share of injected current, the collector current will appear higher than would be expected from the forward active region (see Sec. 2.3). Remember to swap back emitter and collector when done.

4. Before doing column 4, obtain an I_C–V_{EC} plot as follows: Keep $V_{BB} = 4\,\text{V}$ and swap emitter and collector back to the way they were before. Insert $R_A = 10\,\text{k}\Omega$. While sweeping roughly $V_{CC} \in [0, 6]\,\text{V}$, sample and plot I_C vs. V_{EC} for the range $V_{EC} \in [0, 2]\,\text{V}$ (only). You will need to take more data samples at low V_{CC}, where $-\text{d}I_C/\text{d}V_{CC}$ is large; if you require greater resolution in this region, consider using $R_A = 16\,\text{k}\Omega$ (which will yield $V_{EC} \in [0, 0.6]\,\text{V}$ for $V_{CC} \in [0, 6]\,\text{V}$) or $R_A = 20\,\text{k}\Omega$ (yielding $V_{EC} \in [0, 0.2]\,\text{V}$). You may also find it a useful approach to take measurements at evenly spaced values of I_C in this region. (Note this measurement could also be done using the X-Y function of an oscilloscope. Note also that we are holding V_{EB} constant, while we should be fixing I_B. The low sensitivity of I_B to V_{EC} allows us to make this approximation.)

5. Use the plot to determine the Early voltage V_A for this I_B. How well does your value agree with that predicted by the Ebers-Moll model?

6. Leave the setup as it is, find a V_{CC} that will bias the BJT in saturation. Complete column 4 of Table 4 and sketch the simplified Ebers-Moll circuit model.

7. Compare your forward- and reverse-active region results with those from the HP-4155-assisted measurements.

5 Optional Experiments

5.1 Circuit Simulation (Basic)

Using the parameters you have extracted, write a SPICE pnp BJT `.MODEL` card suitable for simulating common-collector configurations, and illustrate its use by using the circuit shown in Fig. 7(b) to simulate the graph of the BJT's I_C–V_{EC} characteristics. You will need to perform a nested sweep, sweeping $V_E \in [0,\, 2.5]\,\mathrm{V}$ and stepping $I_B \in -\{20, 40, \ldots 80\}\,\mu\mathrm{A}$. (Don't bother to try to model the emitter or substrate current accurately.)

References

[1] *HP 4155B/4156B User's Guide: Measurement and Analysis*, 3rd ed., Hewlett Packard, Japan, Oct. 1998. [Online]. Available: http://www.et.fh-muenster.de/research/mmedia/document/hp4155b/download/90200.pdf