Refer to Figure 10.5

\[ A_{in} = \frac{V_{in}}{R_{in} + R_{in}} \times \frac{1}{2 \pi f C_{in}} \]

where

\[ R_{in} = R_{in} \parallel R_{in} = 47 \, \text{M\Omega} \parallel 10 \, \text{M\Omega} = 8.426 \, \text{M\Omega} \]

\[ R_{in} = 100 \, \text{k\Omega}, \quad f_{in} = 5 \, \text{mA/V}, \quad R_{0} = 4.7 \, \text{k\Omega} \parallel 10 \, \text{k\Omega} \]

\[ C_{in} = \frac{1}{2 \pi f_{in} (R_{0} + R_{in})} \]

\[ f_{in} = \frac{1}{2 \pi (R_{0} + R_{in})} \times \frac{1}{2 \pi f_{in} (R_{0} + R_{in})} \]

\[ = \frac{1}{2 \pi} \times \frac{1}{0.01} \times \frac{1}{16.426} + 0.1 \times 10^6 \]

\[ = 1.9 \, \text{Hz} \]

\[ C_{in} = \frac{3.8 \, \text{F}}{2.4 \, \text{F}} \]

\[ f_{in} = \frac{8.426 \, \text{F} 	imes 5.47 \, \text{F}}{2.4 \, \text{F}} \]

\[ = -15.8 \, \text{V} \]

\[ V_{in} = \frac{1}{2 \pi f_{in} (R_{0} + R_{in})} \]

Draw an equivalent circuit (All external coupling/coupled capacitors are shown)

\[ R_{in} = R_{in} \parallel R_{in} = 47 \, \text{M\Omega} \parallel 10 \, \text{M\Omega} = 8.426 \, \text{M\Omega} \]

\[ V_{in} = \frac{1}{2 \pi f_{in} (R_{0} + R_{in})} \]

\[ V_{out} = -V_{out} \frac{1}{8.426 \, \text{M\Omega} + 4.7 \, \text{k\Omega}} \]

\[ \frac{1}{2 \pi f_{in} (R_{0} + R_{in})} \]

Note: If you can also solve for \( R_{in} \) using impedance, you can see that \( R_{in} = R_{in} \parallel R_{in} \) so \( V_{out} = -V_{out} \frac{1}{8.426 \, \text{M\Omega} + 4.7 \, \text{k\Omega}} \). Then you can use the voltage divider to get the input:

\[ V_{in} = \frac{R_{in}}{R_{in} + R_{in}} \]

To minimize capacitance, find the matching point impedance for each cap while shrinking the others.

\[ C_{in} = \frac{1}{2 \pi f_{in} (R_{0} + R_{in})} \]

Since there are no sources in series, \( V_{out} \) is dependent only on \( R_{in} \).
Refer to Example 10.14 → now $I_E$ is decided. In $mA$

$S_n = \frac{I_c}{V_c} = 2 \text{ mA} / 25 \text{ mV} = 80 \text{ mA/V}$

$r_a = \frac{\beta}{S_n} = \frac{100}{80 \text{ mA/V}} = 1.25 \text{ kΩ}$

$r_e = \frac{V_c}{I_c} = \frac{100 \text{ V}}{2 \text{ mA}} = 50 \text{ kΩ}$

$C_e + C_w = \frac{g_m}{2 \pi \times 800 \times 10^6} = 16 \text{ pF}$

$C_T = 1 \text{ pF}$

$C_C = 15 \text{ pF}$

$r_1 = 50 \text{ kΩ}$

$R_o = 50 \text{ kΩ}$

$R_C = 4 \text{ kΩ}$

The new value of $A_{un}$ is

$$A_{un} = r_o - \frac{R_o + R_w}{r_a + r_1 + (R_1 \parallel R_2) (r_o R_t)}$$

where

$$R_1 = r_o \parallel R_C \parallel R_2$$

$$R_w = 50 \parallel 4 \parallel 5 = 2.13 \text{ kΩ}$$

Thus,

$$r_o R_1 = 80 \times 2.13 = 170 \text{ V/V}$$

and

$$A_{un} = \frac{50}{50 + \frac{1.25}{1.25 + 0.05 + 0.05} \times 170}$$

$$= 33 \text{ V/V}$$

and

$$20 \log A_{un} = 30.4 \text{ dB},$$

or previous value of $39 \text{ %}$ ($52 \text{ %}$)

This should be compared to the previous value of $39 \times 754 = 29.4 \text{ MHz}$. Thus, increasing the bias current by a factor of 2 results in an increase in $f_o$ by a factor of 1.16—that is, by about 16%.

However, because of the attendant reduction in input resistance, the overall gain decreased by about the same factor and GB remained nearly constant. The price paid for the slight increase in $f_o$ is an increase in power dissipation by a factor of about two.
**Solve for key points, ensure connections**

\[ V_a = (500k) \left( \frac{1}{5k} \right) = 10V \]

\[ I_a = \frac{V_a}{R_a} = \frac{10}{1k} = 10mA \]

\[ V_{a-b} = \frac{V_a}{R_a} \cdot R_b = 10mA \cdot R_b \]

\[ V_{a-c} = \frac{V_a}{R_a} \cdot R_c = 10mA \cdot R_c \]

\[ \Theta = \frac{1}{R_a} \cdot \left( \frac{1}{R_b} + \frac{1}{R_c} \right) \]

\[ \text{poling:} \quad V_a = \frac{V_{a-b} + V_{a-c}}{2} = \frac{10mA \cdot R_b + 10mA \cdot R_c}{2} = 5mA \cdot (R_b + R_c) \]

\[ R_b = 24 \text{ k}
\]

\[ V_a = 1.95V \]

\[ 0.528V \text{ at } \theta \]

\[ I_b = \frac{V_b}{R_b} = \frac{0.528V}{24k} = 0.022mA \]

\[ V_0 = V_b - V_a = 18 - (0.22mA \times 75k) = 2.52V \]

\[ V_1 = 2.52V \]

\[ V_2 = V_a - V_0 = 10V - 2.52V = 7.48V \]

\[ V_3 = 3.34V \]

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**Find the input & output resistances**

For any JFET devices, terminal resistances for the generally loaded NOSFETs. In the future, these depictions can be used along w injection triangulars.

\[ R_i = \left( \frac{1}{R_a} \right) \left( \frac{1}{R_b} \right) \]

\[ R_i = \frac{R_a + R_b}{R_a R_b} \]

\[ R_i = \frac{R_a}{R_a} + \frac{R_b}{R_b} \]

**Use hybrid v model**

\[ R_{i0} = \frac{R_a}{R_a} + \frac{R_b}{R_b} \]

\[ R_{i0} \approx R_a + \frac{R_b}{R_a} \]

\[ R_{i0} \approx R_a + \frac{V_a}{I_a} \]

\[ R_{i0} \approx R_a + \frac{10V}{10mA} = 1000 \Omega + 2k \Omega = 3k \Omega \]

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**New, find unknown gains: basic flow work**

\[ \text{S.S. circuit} \]

\[ \text{injection} \]

\[ V_{in} = \frac{V_{out}}{AV} = -2.2 \text{V} \]

\[ V_{in} = \frac{V_{out}}{-3.22 \text{V}} = -7.5 \text{V} \]
For $V_{dd}$, consider time constants associated with coupling & bypass caps:

$$\tau_c = R_c \times C_c = (1 \text{ M} \times 600 \text{ nF}) \times (1 \text{ nA}) = 600 \text{ kA}$$

$$\tau_0 = \frac{1}{2\pi f_0} = 0.216 \text{ Hz}$$

$$\tau_1 = \frac{1}{2\pi f_1} = 545 \text{ kHz}$$

$$\tau_2 = \frac{1}{2\pi f_2} = 2.2 \text{ kHz}$$

$$\tau_3 = \frac{1}{2\pi f_3} = 8.5 \text{ kHz}$$

Since there is no dominant pole:

$$f_0 = 4.8 \text{ GHz}$$

$$f_1 = 11.64 \text{ Hz}$$

For $V_{dd}$, consider the time constants associated with internal caps:

- Note that $C_{in}$ is grounded at both terminals, which means it effectively isn't there.
- $C_{in}$ is a Miller capacitor, so as it has gain $-\frac{\partial T}{\partial V_{dd1}} \times \frac{R_C}{R_{dd1}}$ across $R_C$.
- So @ zero we have total effective capacitance $C_{dd1} = C_{dd1} + (1 + \frac{R_{dd1}}{R_C})C_{in} = 1 \times C_{dd1}$.
- To find the effective Miller capacitance on the drain, find the drain-to-gate gain:

$$G_{dd1} = \frac{V_{dd2}}{V_{dd1}} \Rightarrow C_{dd,eq} = \frac{1}{1 + G_{dd1}}C_{dd1}$$

$$C_{dd,eq} = C_{dd1}$$

- Total capacitance @ drain is $C_{dd} = C_{dd1} + C_{dd2} + C_{dd3}$.

Driving gate impedance:

$$R_{dd} = R_{dd1} \times R_{dd2} \times R_{dd3} \times \left( \frac{36}{14} \right) \times \left( \frac{1}{14} \right) = 1 \text{ k}$$

$$C_{dd} = C_{dd1} + C_{dd2} + C_{dd3} \approx 6.2 \text{ fF}$$

$$f = \frac{1}{2\pi R_C C_{dd}} = \frac{1}{(2\pi)(1000 \text{ Ohm}) \times (6.2 \text{ fF})} \Rightarrow f_{min} = 1.2 \text{ GHz}$$

$$f_{50} = \frac{1}{\sqrt{2\pi f_{min}}} = \frac{1}{\sqrt{2\pi \times 1.2 \text{ GHz}}} = 3.9 \text{ GHz}$$

$$f_{3dB} = \frac{1}{2\pi R_C C_{dd}} = \frac{1}{(2\pi)(1000 \text{ Ohm}) \times (6.2 \text{ fF})} \Rightarrow f_{3dB} = 6.3 \text{ MHz}$$

Max input limited by output signal that causes transistor to leave saturation:

$$V_{DD, min} = V_{DD} \times V_{DD, max} = V_{DD} \times (V_{DD1} - V_{DD2}) = (3.3 \text{ V}) \times (1 \text{ V} - 0.9 \text{ V}) = 3.9 \text{ V}$$

$$V_{DD} = V_{DD, min} = 3.3 \text{ V}$$

Max output amplitude is $\frac{V_{DD1}}{2} = 1.65 \text{ V}$

$$V_{DD, max} = \frac{V_{DD1}}{2} = 1.65 \text{ V} \Rightarrow V_{DD, max} \approx 152 \text{ mV}$$
To find additional impact of $R_e$ on gain, draw CL model:

$$v_{OC} = v_o = (3V_R)(50k) = 150V$$

Next, calculate internal capacitor values:

$$C_m = \frac{C_{0m}}{1 + \frac{v_{OC}}{V_{oc}}} = \frac{(14.98 \mu F)}{1 + \frac{150V}{5V}} = 5.5 \mu F$$

$$C_T = 144 \mu F$$

$$C_{oa} = \frac{25 \mu F}{1 + \frac{150V}{5V}} = 8.33 \mu F$$

Several other problems were encountered during the analysis.
\[ C_p = R_C r_{pe} C_{22} = \left[ R_e \times R_{bb} \times (\frac{1}{r_{pe} f_{m}}) \times (R_e + R_L) \right] C_{22} = 119 \text{ ps} \]

\[ f_m = \frac{1}{2\pi \sqrt{C_p,C_{22}}} \Rightarrow f_m \approx 164 \text{ MHz} \]

\[ f_{c1} = \frac{1}{2\pi \sqrt{C_{c1}}} \Rightarrow f_{c1} = 1.03 \text{ Hz} \]

\[ f_{c2} = \frac{1}{2\pi \sqrt{C_{c2}}} \Rightarrow f_{c2} = 0.66 \text{ Hz} \]

\[ f_L = f_{c1} + f_{c2} + f_{r} \Rightarrow f_L \approx 5.7 \text{ Hz} \]