Lecture 39: Complex Circuits & Course Wrap Up

- Announcements:
  - Lab#6 due Friday, 12/11 (last day of RRR week)
  - 2nd Lab#6 Checkpoint due next week (breadboard circuit)
  - Will go through Final Exam Info Sheet today
  - Will also leave some time for Course Evaluations
    - For info on how, go to:
      https://drive.google.com/drive/folders/1aA0OzAk1Rt8DuDE9KSkKiQzN05whZUJ
  - Lecture Topics:
    - Complex Gates
    - Differential Pair (Op Amp)
    - Course Wrap Up
    - Final Exam Info Sheet
    - HKN Evaluations
  - Last Time:
    - Derived CMOS inverter propagation delay
    - Now, look at a more complex gate ...

### Complex CMOS Gater

To realize more complex gaters, use the following structure:

- For CMOS, to save power consumption, must avoid a conductive path connecting $V_{DD}$ and ground in steady-state
- Otherwise, too much current will flow and dissipate power
- Should also minimize this path during transitions

When this network provides a path to $V_{DD}$, the output should be a high or '1'

When this network provides a path to ground, the output should be a low or '0'
**CMOS NOR Gate**

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When both inputs are '0', there should be a path to VDD.

Anytime there is a '1' in the input, need to pull down to GND.

Start w/ Reference CMOS Inverter:

- Assume: \( \mu_nC_{ox} = 2.5 \mu_pC_{ox} \)

NOR Gate:

When \( V_N = V_{oh} \):

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Differential Gain: \( A_d = \frac{N_{d1} - N_{d2}}{N_{id}} = \frac{N_{ad}}{N_{id}} \) (Wont BIG)

Common-Mode Gain: \( A_{cm} = \frac{N_{o1} - N_{o2}}{N_{icm}} \) (Wont BIG)

Common-Mode Rejection Ratio: \( CMRR = \frac{A_{dm}}{A_{cm}} \)

Simple MOS Op Amp

\[ N_0 = \frac{i_{R01} R_{D2}}{1 + \frac{1}{2} g_m N_{S5} R_{D2}} \]

\[ \frac{N_0}{N_S} = \frac{1}{(N_4 - N_2)} \]

Get Gain: \( \frac{N_0}{N_S} = \frac{N_0}{N_4 - N_2} = A_0 \)

Remarks:
1. For more gain, add a common-source stage.
2. For lower \( R_{D1} \), add a common-drain stage.

All these things that you already know!
• What's Next?
• EE130: Semiconductor Devices
  ✈ Did you like the physics parts? If so, then this is the course for you.
  ✈ Will go much deeper and cover
    — Energy band diagrams
    — Short channel MOS
    — More accurate physical structure
    — Heterojunctions
    — Much more …
• EE143: Semiconductor Device Fabrication
  ✈ Planar wafer-level fabrication methods that make IC's possible
  ✈ Tools and chemistry
  ✈ Process flow design
  ✈ Hands-on wafer fabrication
• EE140: Analog Integrated Circuits
  ✈ Supply and temperature independent biasing
  ✈ Much larger circuits
  ✈ Deeper understanding of op amps
  ✈ Stability compensation
  ✈ Feedback methods (by inspection)
• EECS151: Digital Integrated Circuits
  ✈ Build upon propagation delay concepts
    — Short channel devices
    — Logic gates, adders, etc.
  ✈ System-level design
    — Interconnect issues
    — Programmable arrays

• What's Next? (cont.)
• EE147: Microelectromechanical Systems (MEMS)
  ✈ I'm biased, but … this is the coolest stuff, period!
  ✈ Mechanics and Materials
  ✈ Methods for fabricating tiny mechanics
  ✈ Mechanical circuit design
  ✈ You'll learn that all of your EE math skills and circuit techniques can just as easily be applied to mechanical devices and systems
  ✈ Applications to sensing and RF