Lecture 37: Digital Circuits

Announcements:
- HW#11 online and due Friday, 12/4
- Lab#6 online and due Friday, 12/11 (last day of RRR week)
- 1st Lab#6 Checkpoint due this week (spice)

Lecture Topics:
- Active Loads
- Digital Circuits
- CMOS Inverter
  - Voltage Transfer Characteristic
  - Propagation Delay

Last Time:
- Went through MOS inspection analysis
- Now, consider active loads ...

Active loads

\[ V_{DB} \]
\[ V_{RB} \]
\[ \frac{V_{RB}}{V_{DB}} \cdot \frac{I_{D}}{I_{D}} = \frac{2I_{D}R_{D}}{(V_{DB}-V_{T})} = \frac{V_{RB}}{(V_{DB}-V_{T})} \]

Like bipolar, gain is limited by the voltage across \( R_{D} \)

(s.s. C.t.)

To get a better solution: replace \( R_{D} \) w/ a current source

\[ V_{DD} \]
\[ I_{D} \]
\[ V_{ON} \]

Approximate current source w/ a PMOS transistor:

\[ V_{DD} \]
\[ V_{ON} \]
\[ I_{DS} \]

Since \( V_{GS2} = V_{GS3} \)
So far, our focus has been on analog amplifiers that process analog signals.

Earlier in the class, however, we looked at different signal types: analog, sampled-data, and digital.

Digital Signal:

- With enough levels, we can reduce quantization error to unnoticeable levels.
- The process via digital electronics, e.g., adder.

These values can now be encoded in a binary representation and processed via digital electronics.

Problem: Lose information through quantization.

Lost Info $\propto \frac{1}{\# \text{of levels}}$
• This class won't cover the design of this adder
• For now, suffice it to say that one way to design the adder is to put together a circuit of gates: inverters, NAND gates, NOR gates, etc.

- Here, 0 → low voltage, 1 → high voltage
- If you have a NAND gate, you can make any digital function, including the adder above
- The NAND gate is a digital circuit that uses 4 transistors

• The key to understanding this circuit starts with understanding a simpler circuit: the inverter
- $V_{OL} = \text{output low voltage (0)}$
- $V_{OH} = \text{output high voltage (1)}$
- $V_{IL} = \text{max. input voltage recognized as input low}$
- $V_{IH} = \text{min. input voltage recognized as input high}$
- $NM_L = V_{IL} - V_{OL} = \text{noise margin low}$
- $NM_H = V_{OH} - V_{IH} = \text{noise margin high}$

Why noise margins?

![CMOS Inverter Diagram]

1. Case: $V_N < V_{IL}$
   - $M_N$ off, $M_P$ on
   - $V_{OH} = V_{DD}$
   - Eliminates body effect

2. Case: $V_N > V_{IH}$
   - $M_N$ on, $M_P$ off
   - $V_{OL} = 0V$
   - $NMOS$ discharges $C_L$ to

Get $V_{OH}$ & $V_{OL}$:

- $V_{OL} = 0V$
- $V_{OH} = V_{DD}$
Voltage Transfer Characteristic for CMOS

\[ V_{TH} = \frac{5V_{DD} + 3V_{TN} + 3V_{TP}}{8} \]

\[ V_{IL} = \frac{2V_{DD} + 5V_{TN} + 3V_{TP}}{8} \]

Dynamic Behavior of the CMOS Inverter

Propagation Delay:

\[ t_p = \text{avg. propagation delay} = \frac{t_{PHL} + t_{PLH}}{2} \]

\( t_{PHL}, t_{PLH} \) gives a value for the delay across this two-stage inverter chain.
• Remarks
  • Propagation delay is the delay experienced by a signal passing through a gate as measured between the 50% transition points between input and output waveforms.
  • In general, a gate displays different response times for rising and falling input waveforms.
  • Thus, define:
    \[ t_{pLH} \]: response time of a gate making a low \( \rightarrow \) high output transition.
    \[ t_{pHL} \]: response time of a gate making a high \( \rightarrow \) low output transition.
  • Propagation delay then defined as the average of \( t_{pLH} \) and \( t_{pHL} \).
  • What causes switching delay?
    \[ \text{Finite current transistor current drive (i.e., finite on resistance } R_{on} \text{)} \]
    \[ \text{Output node capacitance} \]

Actual CMOS (old) (an inverter)