I. Lab 6 Extension – **Now due Saturday, 12/12/20 @ midnight**

II. 2019 Final Exam
Problem 1. Total 20 points

This problem considers the DC biasing of the 4-stage amplifier circuit shown below with element values and transistor parameters. (You will not be asked to do any small-signal analysis.) Find the DC voltage $V_{BE}$ at the emitter of transistor $Q_1$ for $R_1=4\,\Omega$ and $R_2=210.5\,\Omega$. Note that some of the transistors may not be operating in the forward active region.

For all transistors:

$\beta = 200, V_{BE(on)} = 0.7V, V_{BE(on)} = 0.8V, V_{CE(on)} = 0.2V, V_T = 200V, V_T = 25\,mV$

In solving this problem, you may use approximations where applicable, but be careful. Your answer is correct if it is within 5% of the correct answer.
Fall 2019 Final | Problem 1

\[ V_{CE2} = 0.7V > V_{CE, sat} \Rightarrow Q_2 \text{ in F.A. } \checkmark \]

Still assuming \( Q_3 \) in F.A.

\[ I_{E3} = \frac{9.6V}{1k\Omega} = 9.6 \text{ mA} \]

\[ V_{C3} = V_{CE} - I_{C3} R_{C3} = 10 - (9.6 \text{ mA})(5k\Omega) = -33V < V_{CE(sat)} \]

\( \Rightarrow Q_3 \text{ is in saturation!} \)

\( \because I_{C3} \neq I_{E3}, \quad V_{CE3} = V_{CE(sat)} = 0.2V \)

\[ V_{BE3} = V_{BE(sat)} = 0.8V \]

\[ V_{E3} = 8.5V \Rightarrow V_{C3} = V_{E3} + V_{CE(sat)} = 8.7V \]

\[ V_{CE4} = 10 - 8 = 2.0V > V_{CE(sat)} \text{ confirms F.A.,} \]

For all transistors:

\( \beta = 200, V_{BE(on)} = 0.7V, V_{BE(sat)} = 0.8V, V_{CE(sat)} = 0.2V, V_T = 25mV \)

Assume \( Q_4 \) in F.A. \( V_{E4} = V_{C3} - V_{BE(on)} = 8.0V \)

\( V_{CE4} = 10 - 8 = 2.0V > V_{CE(sat)} \)
For all transistors:

$\beta = 200$, $V_{BE(on)} = 0.7 \text{V}$, $V_{BE(sat)} = 0.8 \text{V}$, $V_{CE(sat)} = 0.2 \text{V}$, $V_A = 200 \text{V}$, $V_T = 25 \text{mV}$
**Problem 2**: Total 80 points

This problem involves the BiCMOS amplifier circuit shown below, together with relevant data for devices.

![BiCMOS Amplifier Circuit](image)

**Device Parameters:**
- npn BJT: $V_I = 25\text{mV}$, $V_{BEB(off)} = 0.7V$, $V_{BEB(on)} = 0.8V$, $V_{CE(off)} = 0.2V$, $\beta = 200$, $V_i = 200V$
- Base Doping Conc. = $N_{A_B} = 10^{17} \text{cm}^{-3}$, Collector Doping Conc. = $N_{A_C} = 10^{18} \text{cm}^{-3}$
- Collector-Base Overlap Area = $60 \times 45 \mu\text{m}^2$, $f_T = 400\text{MHz}$
- NMOS: $V_{TN} = 0.7V$, $2\phi_i = 0.6V$, $K_s = 30\mu\text{A/V}^2$, $\lambda_n = 0 \text{ V}^{-1}$, $\gamma_n = 0 \text{ V}^{-1/2}$

Answer the following questions regarding this circuit.

(a) Determine the value of $R_E1$ that sets the collector current of $Q_1$ to 1mA.

For the rest of this problem, assume the collector current of $Q_1$ is 1mA and the drain current of $M_2$ is 0.7mA.

(b) Write an expression for the input resistance $R_i$ and provide a numerical value.

(c) Write an expression for the output resistance $R_o$ and provide a numerical value.

(d) Write an expression for the mid-band gain ($v_o/v_i$) and provide a numerical value.

(e) Write an expression for the upper cut-off frequency in terms of small-signal parameters.

(f) Calculate the zero-bias base-to-collector junction capacitance $C_{ij}$ for $Q_1$.

(g) Calculate the contribution to the high frequency time constant from the node at the base of $Q_1$. 

(a) $I_{C1} = 1mA = I_{E1} = \frac{V_{E1}}{R_{E1}}$

$V_{B1} \approx V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} = 5.33V$

$R_{E1} = \frac{V_{E1}}{I_{C1}} = \frac{4.63}{1mA}$

$b) \ R_{in} \ @ \ text{mid band}$

- $C_{E1}$ short $R_{E1} \rightarrow$ C.E. $\rightarrow R_b = \beta_{200}$

- $R_{in} = \frac{R_1 R_2}{R_B} R_{\beta}$

- $r_{\beta_{200}} = \frac{200}{9m_1}, m_1 = \frac{I_{C1}}{V_T}, V_T = 25mV$

$R_{in} = 4.082k\Omega$
\( I_{D2} = 0.7 \text{mA (given)} \)

(c) \( R_{out} = ? \) @ midband

For MOSFET \( \beta = \frac{I_D}{I_G} = \frac{V_D}{I_G} = \infty \)

\[
R_s = \frac{\alpha}{g_m 2} = \frac{1}{g_m 2} \quad \text{where} \quad \alpha = 1
\]

\[
R_{out} = R_{S2A} || \left( \frac{1}{R_{S2B} + \frac{1}{g_m 2}} \right)
\]

\[
g_m = \frac{2I_{D2}}{V_D} = \sqrt{2f_{DM} \cdot \lambda_2 (W/L)^2} = 2.05 \times 10^{-4} \text{ S}
\]

\[
R_{out} = 696 \Omega
\]

Device Parameters:
- npn BJT: \( V_t = 25 \text{mV}, V_{BE(on)} = 0.7 \text{V}, V_{BE(off)} = 0.8 \text{V}, V_{CE(sat)} = 0.2 \text{V}, \beta = 200, V_a = 200 \text{V} \)
- Base Doping Conc. = \( N_a = 10^{17} \text{ cm}^{-3} \), Collector Doping Conc. = \( N_c = 10^{15} \text{ cm}^{-3} \)
- Collector-Base Overlap Area = \( 60 \times 45 \text{ \mu m}^2 \), \( f_t = 400 \text{MHz} \)
- NMOS: \( V_{TH} = 0.7 \text{V}, 2|\phi| = 0.6 \text{V}, K_o = 30 \mu \text{A/\text{V}^2}, \lambda = 0 \text{ V}^{-1}, \gamma = 0 \text{V}^{-1/2} \)
\( \frac{\Delta V_o}{\Delta V_S} = \frac{\mu b_1 \cdot V_{C1} \cdot \Delta V_S}{\beta_1 \cdot V_{C1} \cdot \Delta V_S} \)

\( = \left( \frac{R_{in}}{R_{in} + R_S} \right) \left( -g_{m1}(R_{c1}||R_0) \right) \left( G_{m2} \cdot R_S \right) \left( \frac{R_{S2B}}{R_{S2A} + R_{S2B}} \right) \left( \frac{1}{R_{S2B}} \right) \)

\( = \frac{9}{1 + g_{m2}R_S} \)

\( V_{o} = -185 \text{ V/V} \)

\( C_{MO} = \frac{e_{si}A_o}{\chi d_o} = \frac{(11.7)(8.85 \times 10^{-12} \text{ F})}{(60 \mu \text{m} \times 45 \mu \text{m})} \)

\( \chi d_o = \sqrt{\frac{2eS}{q} \left( \frac{1}{N_{AB}} + \frac{1}{N_{OC}} \right)} \phi_j = 0.32 \mu \text{m} \)

\( \phi_j = \frac{kT}{q} \ln \left( \frac{N_{AB}N_{OC}}{n_i^2} \right) = 0.73 \text{ V} \cdot C_{MO} = 0.89 \text{ pF} \)
(e) $f_H = ?$ [expression]

$\tau_0 = \left[ C_m (1 + g_m R_{C1}) + C_{gs1} \right] (R_S \parallel R_{in})$

$\tau_0 = \left( C_m + C_{gs1} + C_{gd2} \right) (R_{C1} \parallel R_{in})$

$\tau_0 = C_{gs2} \cdot \left( \frac{1}{g_m + g_m + g_{nb2}} \right) \left( R_S \parallel R_{S2A} + R_{S2B} \right)$

$C_{gs2} = C_{gs2} \cdot R_{gso} = C_{gs2} \left[ \frac{1}{g_m R_{S2A} + R_{S2B}} \right]$

same as $R_{110}$ but for MOS

$f_H = \frac{1}{2 \pi \left( \tau_0 + \tau_2 + \tau_3 + \tau_{gs2} \right)}$
This problem considers the combined analog/digital circuit below (called a current-starved inverter), where the (W/L) ratios given are in microns and device data is provided in the box below. Here, $M_1$ and $M_2$ behave like switches, which for the purposes of this problem you can treat as ideal. Also, you can ignore Body effect and transistor intrinsic capacitors.

**Device Parameters:**

- **NMOS:**
  - $V_{Tn} = 0.7V$
  - $\mu_C \cdot W = 200 \mu A/V^2$
- **PMOS:**
  - $V_{TP} = 0.7V$
  - $\mu_C \cdot W = 100 \mu A/V^2$

Determine the value of $R_{REF}$ that gives an output high-to-low propagation delay $t_{PHL} = 20ns$ when the input voltage $V_i$ goes from 0V to 3V.
This problem considers the combined analog/digital circuit below (called a current starved inverter), where the \( W/L \) ratios given are in microns and device data is provided in the box below. Here, \( M_1 \) and \( M_2 \) behave like switches, which for the purposes of this problem you can treat as ideal. Also, you can ignore Body effect and transistor intrinsic capacitors.

### Device Parameters:
- **NMOS:**
  - \( V_{TN} = 0.7V \)
  - \( \mu_nC_{ox} = 200\mu A/V^2 \)
- **PMOS:**
  - \( V_{TP} = 0.7V \)
  - \( \mu_pC_{ox} = 100\mu A/V^2 \)

Determine the value of \( R_{REF} \) that gives an output high-to-low propagation delay \( \tau_{H-L} = 20\text{ns} \) when the input voltage \( V_i \) goes from 0V to 3V.

\[
I_{ref} = 75\mu A = \frac{V_{ref}}{R_{ref}} \\
I_{ref} = (V_{DD} - V_{S46} - V_{GSS} - V_{EE}) \\
R_{ref} = \frac{V_{DD} - |V_{GSS}| - V_{GSS}}{I_{ref}} = 5k\Omega \ \\
V_{GSS} = U_{TN} + \sqrt{\frac{2I_{ref}}{\mu_nC_{ox}(\frac{W}{L})}} = 1.31V \ \\
(V_{G46}) = |V_{TP}| + \sqrt{\frac{2I_{ref}}{\mu_pC_{ox}(\frac{W}{L})}} = 1.31V
\]
This problem considers the combined analog/digital circuit below (called a current starved inverter), where the \((W/L)\) ratios given are in microns and device data is provided in the box below. Here, \(M_1\) and \(M_2\) behave like switches, which for the purposes of this problem you can treat as ideal. Also, you can ignore Body effect and transistor intrinsic capacitors.

**Device Parameters:**
- **NMOS:**
  - \(V_{TH} = 0.7\)V
  - \(\mu_C C_{on} = 200\)\(\mu\)A/V\(^2\)
- **PMOS:**
  - \(V_{TH} = 0.7\)V
  - \(\mu_C C_{on} = 100\)\(\mu\)A/V\(^2\)

Determine the value of \(R_{REF}\) that gives an output high-to-low propagation delay \(t_{PHL} = 20\)ns when the input voltage \(V_I\) goes from 0V to 3V.
Problem 4. Total 35 points

This problem considers the circuit below, where the (W/L) ratios given are in microns and device data is provided in the box below. Assume the op amp is ideal and ignore Body effect.

Answer the following questions regarding this circuit.

(a) What is the voltage $V_B$? Check negative f. b. $w_{V_B} = V_{DD} - V_A = 1.3 \, V$

(b) Determine the value of $R_{REF}$ that attains $I_{REF}=25 \, \mu A$.

(c) Assuming $I_{REF}=25 \, \mu A$, write an expression for and provide a numerical value for the small-signal gain from $v_{\text{in}}$ to $v_{\text{out}}$ with $V_O = 0 \, V$.

\[
I_{\text{ref}} = \frac{V_{\text{ref}}}{R_{\text{ref}}} = \frac{V_{\text{DD}} - V_{SD} - V_{eq} - V_{SS}}{V_{B}} \quad \Rightarrow \quad R_{\text{ref}} = 8.08 \, k\Omega
\]

\[
V_{GS} = V_{TM} + \sqrt{\frac{2I_{\text{ref}}}{k_n}} = 0.78 \, V
\]
(c) \[ V_{G1G} = [V_{TP}] + \frac{2I_{ref}}{k_P} = 1.4 \text{V} \Rightarrow V_{OV6} = 1.4 [V_{TP}] = 0.7 \text{V} \]

\[ \Rightarrow \text{M}_2 \text{ & } \text{M}_4 \text{ are also in linear region} \]

\[ \text{A source voltages as } \text{M}_6 \]

\[ R_d4 = \frac{M_P C_{ox} (W/L) (1V_{GSS} - [V_{TP} - V_{DS6}])}{2I_{ref} v_{sd4}} \]

\[ = 8.695 \text{ k}\Omega \]

\[ \frac{V_0}{V_{11}} = -\frac{1}{2} g_m R_d4 = 3.89 \text{ V/V} \]

\[ g_m = 9 \text{ mS} = \sqrt{2 \mu_n C_{ox} (W/L) I_{ref}} = 8.94 \times 10^{-4} \text{ S} \]
Device Parameters:

NMOS:
- $V_{th} = 0.7\text{V}$
- $\mu_nC_{ox} = 200\mu\text{A}/\text{V}^2$
- $\lambda_n = 0.05 \text{ V}^{-1}$

PMOS:
- $V_{th} = -0.7\text{V}$
- $\mu_pC_{ox} = 100\mu\text{A}/\text{V}^2$
- $\lambda_p = 0.1 \text{ V}^{-1}$
**Fall 2019 Final | Problem 4**

---

**Device Parameters:**

**NMOS:**
- $V_{in0} = 0.7V$
- $\mu_0C_{ox} = 200 \mu A/V^2$
- $\lambda_n = 0.05 \text{ V}^{-1}$

**PMOS:**
- $V_{ip0} = -0.7V$
- $\mu_P C_{ox} = 100 \mu A/V^2$
- $\lambda_p = 0.1 \text{ V}^{-1}$

---

$V_{SS} = -1.5V$

---

$V_{DD} = 1.5V$

---

$V_A = 0.2V$

---

Diagram of the circuit with nodes labeled and device parameters.