EE 105 Discussion 6

K. Peleaux & Qiutong Jin
Today

- Exercise 1: S&S 2.93
- Exercise 2
- Exercise 3
- Exercise 4
**2.93** Derive the transfer function of the circuit in Fig. P2.93 (for an ideal op amp) and show that it can be written in the form

\[
\frac{V_o}{V_i} = \frac{-R_2/R_1}{[1 + (\omega_1/j\omega)][1 + j(\omega_2/\omega_2)]}
\]

where \(\omega_1 = 1/C_1 R_1\) and \(\omega_2 = 1/C_2 R_2\). Assuming that the circuit is designed such that \(\omega_2 \gg \omega_1\), find approximate expressions for the transfer function in the following frequency regions:

(a) \(\omega \ll \omega_1\)

(b) \(\omega_1 \ll \omega \ll \omega_2\)

(c) \(\omega \gg \omega_1\)

Use these approximations to sketch a Bode plot for the magnitude response. Observe that the circuit performs as an amplifier whose gain rolls off at the low-frequency end in the manner of a high-pass STC network, and at the high-frequency end in the manner of a low-pass STC network. Design the circuit to provide a gain of 40 dB in the “middle-frequency range,” a low-frequency 3-dB point at 200 Hz, a high-frequency 3-dB point at 200 kHz, and an input resistance (at \(\omega \gg \omega_1\)) of 2 kΩ.
Use these approximations to sketch a Bode plot for the magnitude response. Observe that the circuit performs as an amplifier whose gain rolls off at the low-frequency end in the manner of a high-pass STC network, and at the high-frequency end in the manner of a low-pass STC network. Design the circuit to provide a gain of 40 dB in the “middle-frequency range,” a low-frequency 3-dB point at 200 Hz, a high-frequency 3-dB point at 200 kHz, and an input resistance (at $\omega \gg \omega_1$) of 2 kΩ. Assume $W_2 \gg W_1$.

Bode Plot (Gain plot): 

1. $w \ll W_1$:
   \[ \frac{V_o}{V_i} = -\frac{R_2}{R_1} \]
   \[ \Rightarrow \frac{V_o}{V_i} = -\frac{R_2}{R_1} \]

2. $W_1 \ll w \ll W_2$:
   \[ \frac{V_o}{V_i} = -\frac{R_2}{R_1} \]

3. $w \gg W_2$:
   \[ \frac{V_o}{V_i} = -\frac{R_2}{R_1} \]

\[ A = \frac{A_0}{1 + \frac{w}{W_1}} \]
\[ \text{pole: } W_1 \]
\[ \text{zero: } 0 \]

\[ \left| \frac{V_o}{V_i} \right| \text{ (dB)} \]

-20 dB/dec
Use these approximations to sketch a Bode plot for the magnitude response. Observe that the circuit performs as an amplifier whose gain rolls off at the low-frequency end in the manner of a high-pass STC network, and at the high-frequency end in the manner of a low-pass STC network. Design the circuit to provide a gain of 40 dB in the “middle-frequency range,” a low-frequency 3-dB point at 200 Hz, a high-frequency 3-dB point at 200 kHz, and an input resistance (at $\omega \gg \omega_1$) of 2 kΩ.

$$R_{in} = \frac{1}{\omega C_1 + R_1} \approx R_1$$

$$i_x = \frac{V_x - V_1}{j\omega C_1 + R_1}$$

$$i_x = \frac{V_x}{j\omega C_1 + R_1}$$

$$\Rightarrow \frac{R_2}{R_1} \approx 100$$

$$w_1 = \frac{1}{R_1 C_1} = 2\pi \cdot 200 \text{Hz}$$

$$w_2 = \frac{1}{R_2 C_2} = 2\pi \cdot 200 \text{kHz}$$

$$R_1 = R_{in} = 2 \text{kΩ}$$

$$R_1 = 2 \text{kΩ}$$

$$R_2 = 200 \text{kΩ}$$

$$C_1 = 0.4 \mu F$$

$$C_2 = 4 \text{pF}$$
Exercise 2

The waveform of the input voltage $v_s$ to the circuit below is a square wave with a peak voltage of $1V$ and a period of $T$. Sketch the waveform of the output voltage $v_o$.
Exercise 2

precision rectifier
Exercise 3

The output characteristics for a PMOS transistor are given. What are the values of $K_p$ and $V_{TP}$ for this transistor? Is this an enhancement-mode or depletion-mode transistor?

\[ V_{BD} = V_{SG} + V_{EP} \]

\[ 4.2V = 5V + V_{EP} \]
\[ \Rightarrow V_{EP} = 4.2V - 5V = -0.8V \]

\[ K_p = \frac{M_p \cdot W}{L} \]

\[ Z_{saturation} = \frac{K_p}{2} \left( V_{SG} + V_{EP} \right)^2 \]

\[ 4000 \times 10^{-6} = \frac{K_p}{2} (5V - 0.8V)^2 \]
\[ \Rightarrow K_P = 4.53 \times 10^{-4} \]
Exercise 4

5.57 For each of the circuits shown in Fig. P5.57, find the labeled node voltages. The NMOS transistors have $V_t = 0.9$ V and $k_n'(W/L) = 1.5$ mA/V$^2$.

\[ \frac{\mu_n C_{ox} W}{2} = 1.5 \times 10^{-3} \text{ A/V}^2 \]

\( V_{GS} = V_O \)

\( V_{DS} > V_{GS} - V_{ON} \) (saturated)

\( < V_{GS} - V_{ON} \) (linear)

\( V_{DS} = V_{GS} > V_{GS} - V_{ON} \)

\[ I = \frac{\mu_n C_{ox} W}{2L} (V_{DS} - 0.9)^2 \]

\( V_4 = \frac{5V + 0V}{2} = 2.5V \)

\( V_5 = V_5 = \frac{1kV}{2} \)

\[ V_5 = \frac{\mu_n C_{ox} W}{2L} (V_4 - V_5 - 0.9)^2 \cdot 1k\Omega \]

\[ V_5 = \frac{\mu_n C_{ox} W}{2L} (2.5 - V_5 - 0.9) \cdot 1000 \]

\( \Rightarrow V_5 = 0.66V \)
Exercise 4

5.57 For each of the circuits shown in Fig. P5.57, find the labeled node voltages. The NMOS transistors have $V_t = 0.9\ \text{V}$ and $k_n' (W/L) = 1.5\ \text{mA/V}^2$. 