EE 105 | Discussion 4

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Discussion Outline

• Offset current (i.e., what happens when we have different input bias currents on each input?)
• Design constraint
Recap: the model for input bias current

\[ I_{bias,1} = I_{bias,2} \]
Last week, we found out we could compensate for this bias current—*this only works if the currents are matched!*

\[ R_b = R_1 || R_2 \]

\[ I_{\text{bias},1} = I_{\text{bias},2} \]

\[ R_1 = 10 \, \text{k}\Omega \]

\[ R_2 = 1 \, \text{M}\Omega \]

Common mode:

\[ I_B = \frac{2I_{\text{bias},1} + I_{\text{bias},2}}{2} \]

Offset current:

\[ I_{\text{os}} = I_{\text{bias},1} - I_{\text{bias},2} \]

\[ v_o = 0 \]
Now, consider an offset current that is 10% of $I_{bias,1}$

→ What’s the resulting $v_o$ (ignoring any $V_{OS}$)?

Superpositions:

1. $I_{bias,2} = I_{bias,1}$

$v_i$ $R_b = R_1 || R_2$

$V_o = 0\,\text{V}$

$R_1 = 10\,\text{k}\Omega$

$R_2 = 1\,\text{M}\Omega$

$I_{bias,1} = 200\,\text{mA}$

$1.1 \cdot I_{bias,1} = I_{bias,2}$
Now, consider an offset current that is 10% of $I_{bias}$ → What’s the resulting $v_o$ (ignoring any $V_{OS}$)?

\[ v_o = 0 \, \text{V} + 200 \, \text{mA} \times 0.1 \times 1 \, \text{mV} = 20 \, \text{mV} \]

\[ R_b = R_1 || R_2 \]

\[ R_1 = 10 \, \text{k}\Omega \]

\[ R_2 = 1 \, \text{M}\Omega \]

\[ 1.1 \cdot I_{bias,1} = I_{bias,2} \]
Now include previous $V_{\text{os}} = 2 \text{ mV}$ & $I_{\text{os}} = 0.1 \cdot I_{\text{bias}}$ to find the worst-case dc voltage at the output in this compensated circuit.

1. $V_{\text{os}}$:
   - Gain: Close-loop op amp
   - $V_{\text{os}} = 2\text{ mV}$
   - $V_0 = A \cdot V_{\text{os}} = 2\text{ mV} \cdot 100 = 200\text{ mV}$

2. $I_{\text{os}}$:
   - $V_0 = 20\text{ mV}$
   - Final $V_0 = V_{0,1} + V_{0,2} = 200\text{ mV} + 2\text{ mV} = 220\text{ mV}$
Constrained Op Amp Design

Let’s look at how you might be constrained by a COTS (commercial off-the-shelf) part when trying to design a circuit

- $f_t = 20 \text{ MHz}$
- Slew rate, $\text{SR} = 10 \frac{V}{\mu s}$
- Output saturation, $V_{o,max} = 10 V$
Constrained Op Amp Design

Using the noninverting configuration with

- \( A_v = 10 \frac{V}{V} \)
- \( v_i = 0.5 \text{ V} \)

- \( f_t = 20 \text{ MHz} \)
- \( \text{SR} = 10 \frac{V}{\mu s} \)
- \( V_{o,\text{max}} = 10 \text{ V} \)

What's the maximum frequency signal that can be amplified before output distortion occurs?

\[ v_o = V_o \sin(\omega t) \]

\[ f \geq \frac{\text{SR}}{\pi} \]

\[ V_o = V_i \cdot A_v = 10 \cdot 0.5 = 5 \text{ V} \]

\[ 10 \frac{V}{\mu s} \geq f \cdot 0.5 \]

\[ f = 20 \text{ kHz} \]

\[ f_{-3dB} = 10 \text{ kHz} \]

\[ f_{-20dB} = 2 \text{ kHz} \]
Constrained Op Amp Design

Using the noninverting configuration with

- \( f = 200 \text{ kHz} \)
- \( A_v = 10 \frac{V}{V} \)
- \( f_t = 20 \text{ MHz} \)
- \( \text{SR} = 10 \frac{V}{\mu s} \)
- \( V_{o,max} = 10 \text{ V} \)

What's the maximum input signal amplitude that can be amplified before output distortion occurs?

\[
V_i = 7.96 \text{ mV}
\]

\[
V_o = 796 \text{ mV} \cdot A_v = \frac{7.96 \text{ V}}{10} \leq V_{o,max} = 10 \text{ V}
\]
Constrained Op Amp Design

Using the noninverting configuration with

- \( f = 50 \text{ kHz} \) \( \Rightarrow \) \( A_v = 10 \)
- \( f_t = 20 \text{ MHz} \)
- \( \text{SR} = 10 \frac{V}{\mu s} \)
- \( V_{o,\text{max}} = 10 \text{ V} \)

What's the useable input voltage range?

- \( V_{o,\text{max}} = 10 \text{V} \)
- \( \frac{V_{o,\text{max}}}{A_v} = 10 \)
- \( V_{i,\text{max}} = \frac{V_{o,\text{max}}}{10} = 1 \text{V} \)
- \( 0 \text{V} < V_i < 1 \text{V} \)