IC Fabrication Technology

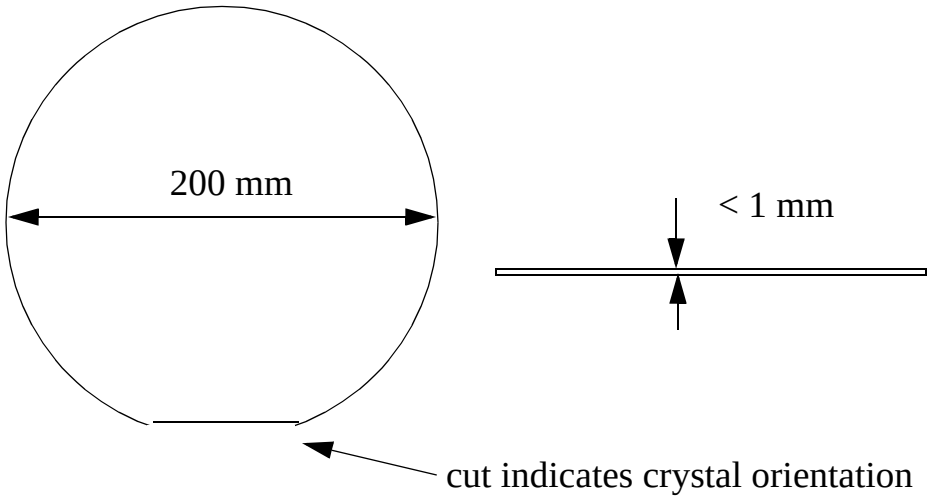
* History:

  1958-59: J. Kilby, Texas Instruments and R. Noyce, Fairchild

* Key Idea: *batch fabrication* of electronic circuits

  An entire circuit, say 10^7 transistors and 5 levels of wiring -- can be made in and on top of a silicon crystal by a series of process steps similar to printing. More than 100 copies of the circuit are typically made at the same time.

  The silicon crystal is called a *wafer*.

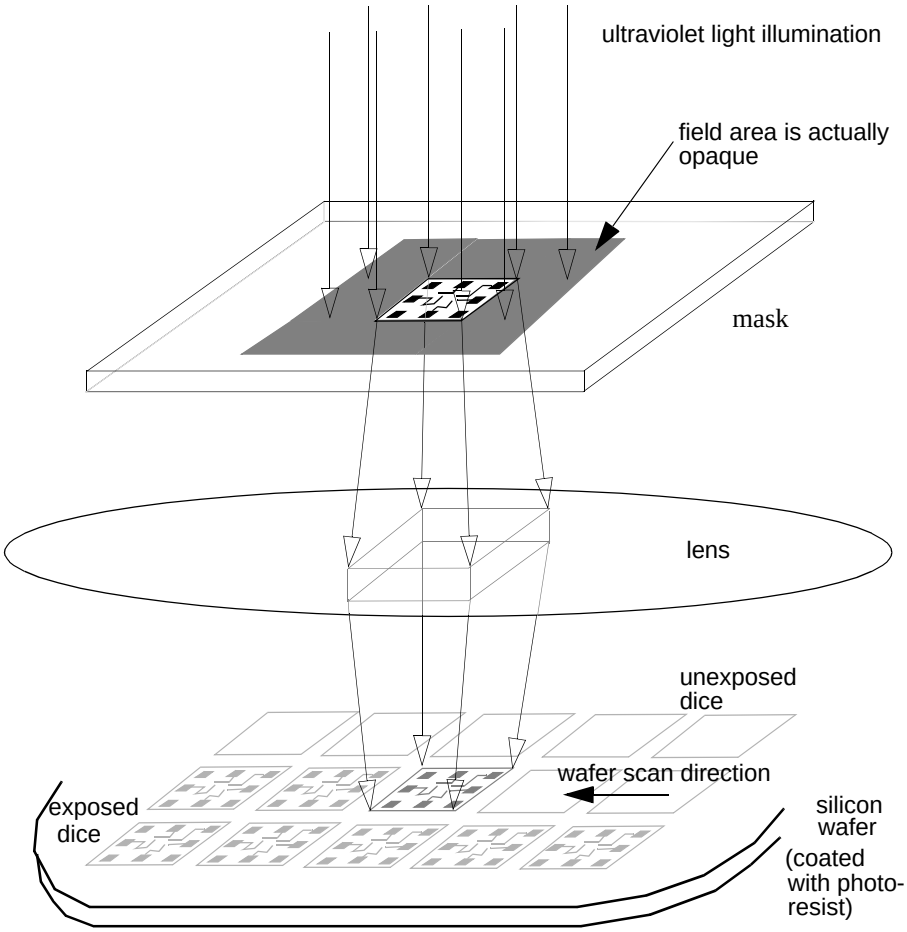


* Results:

1. Complex systems can be fabricated reliably
2. Cost per function drops as the process improves (e.g., finer printing), since the cost per processed wafer remains about the same

Lithography: the Wafer Stepper

The mask is imaged on a photosensitive film (photoresist) that coats the wafer and then the wafer is scanned ("stepped") to the next position



Mask pattern is aligned automatically to patterns on the underlying layers, to a precision of < 0.1 micron.

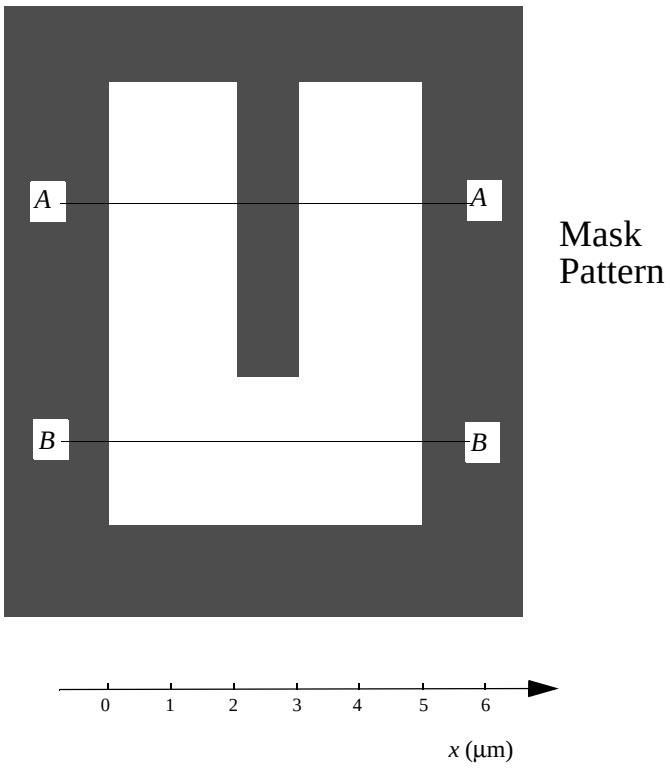
Lithography:
Exposure, Development, and Pattern Transfer

* Simple example of a *mask layout* and a *process* (or *recipe*)

  * *Mask layout* is the set of patterns on the glass plates for patterning the layers (one in this case)

  * *Process* is the sequence of fabrication steps

* Visualize by generating *cross sections* through the structure as it is built up through the process



Photolithography Process

* Photoresist dissolves in alkaline solutions (called “developer”) when it has been exposed to UV light (*positive* photoresist)
* Pattern transfer “subroutine”

  0. Clean wafer

  1. Spin-coat the wafer with 1 μm of photoresist; pre-bake to drive off solvents

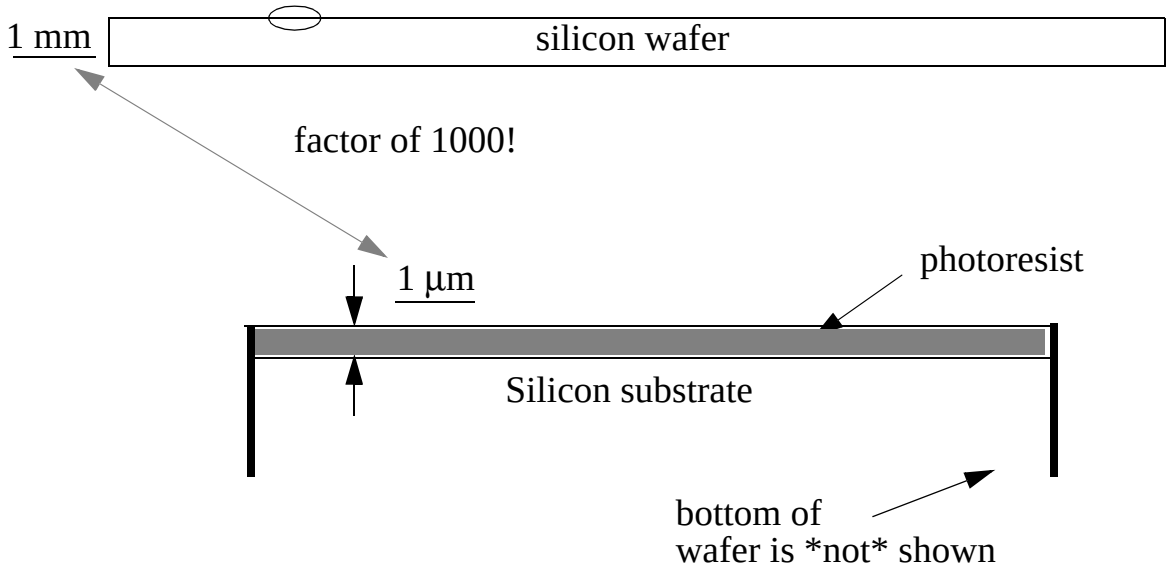
  2. Expose the wafer in the wafer stepper

  3. Develop the image, bake the resist to toughen it against etching

  4. Transfer pattern to underlying film by selectively etching it*

  5. Remove photoresist using an oxygen plasma or organic solvents

* subtractive patterning process (usual case -- EE 105)

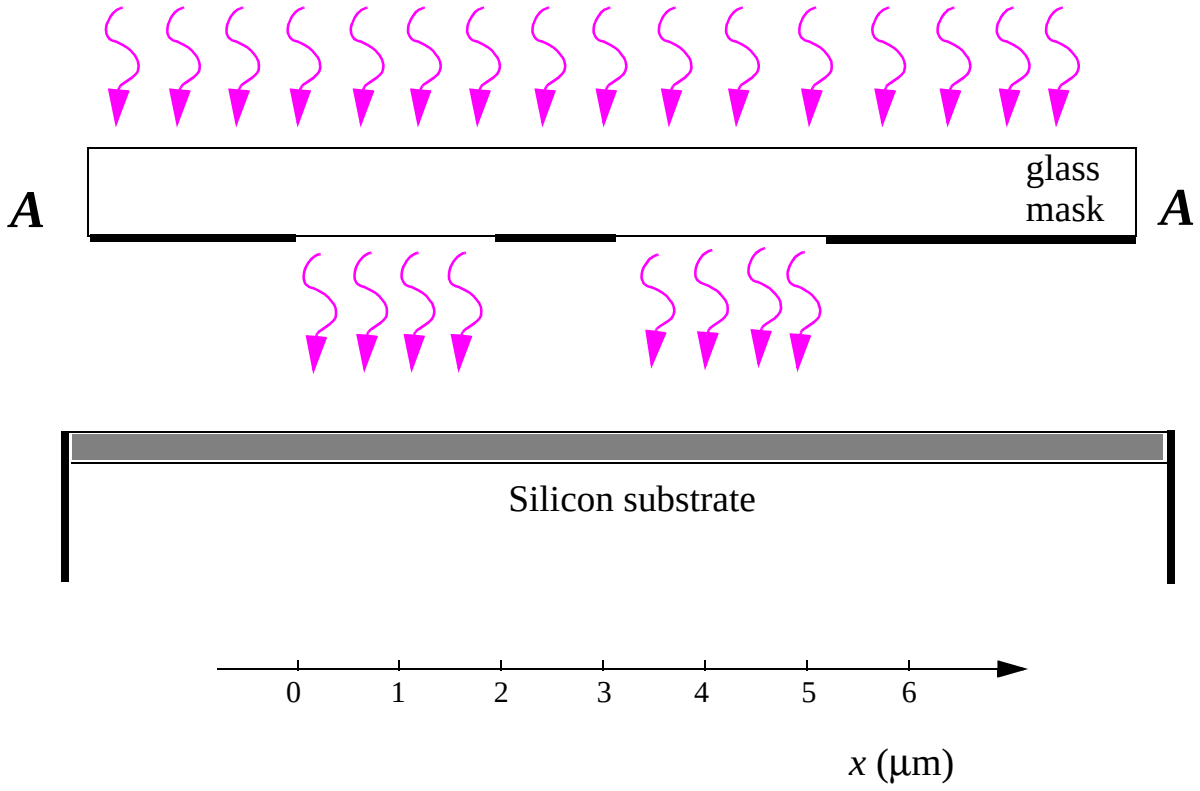


Visualizing Exposure

Omit lens and show UV light going through mask onto wafer

Two-dimensional cross sections are easier than 3D perspective views (for most)

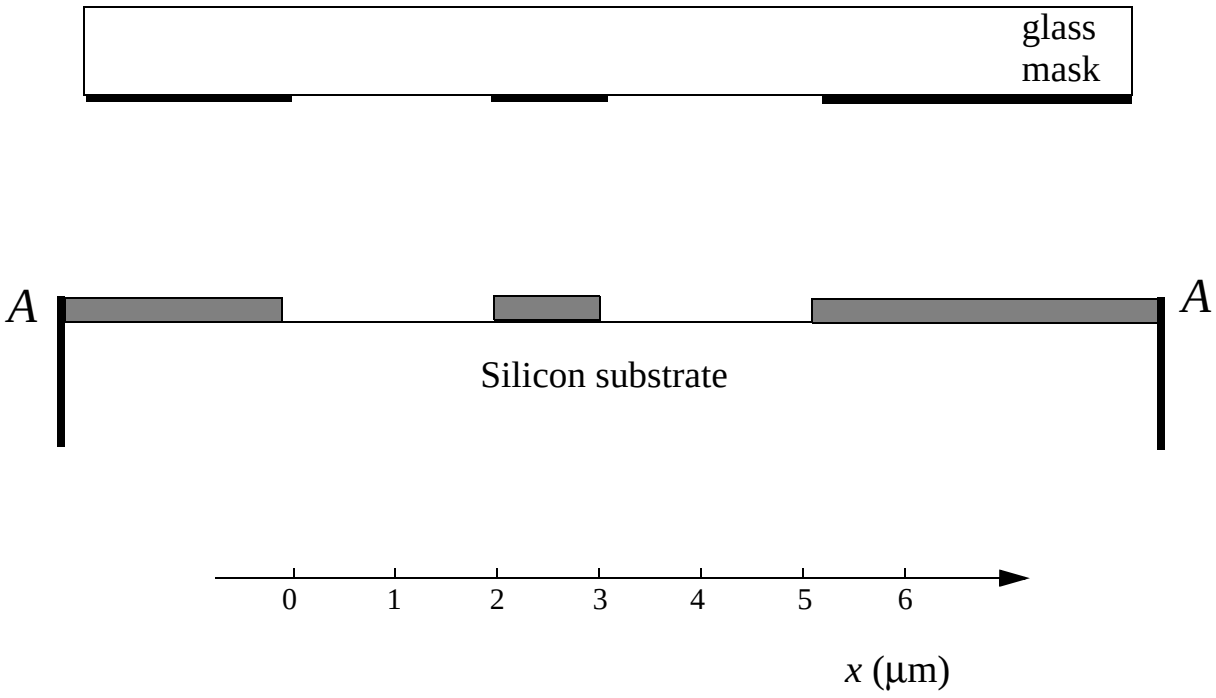
A-*A* cross section



Development

Two-dimensional cross sections are easier than 3D perspective views (for most)

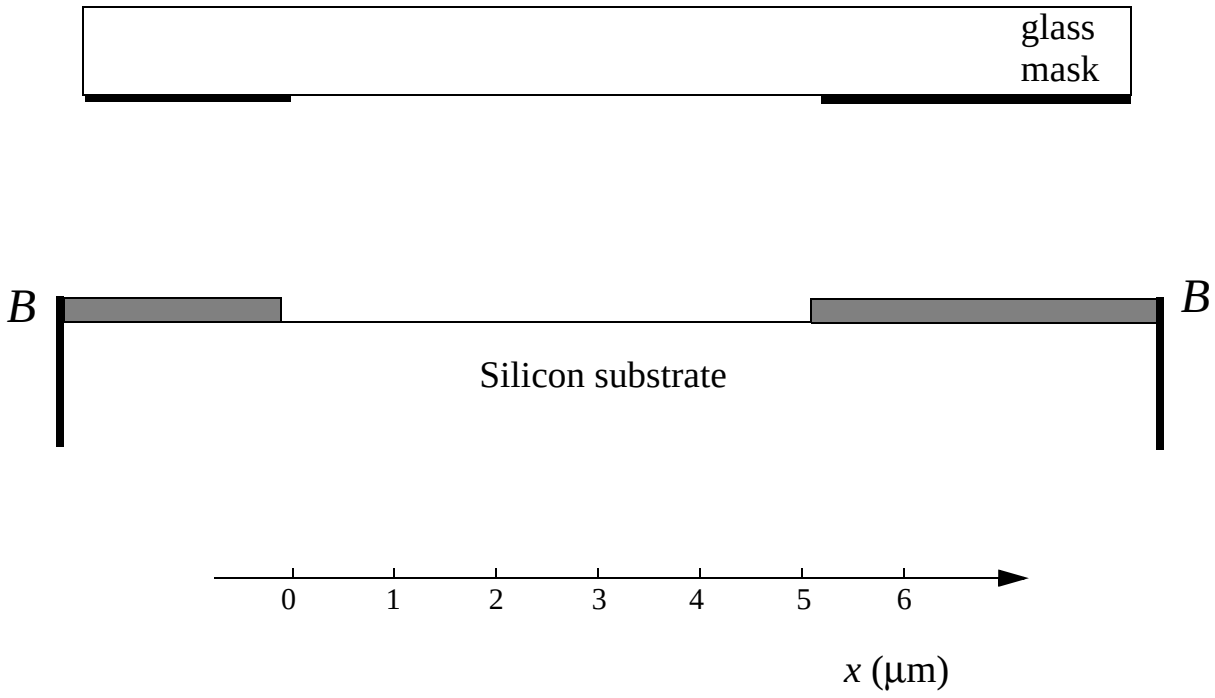
A-*A* cross section



Development

Two-dimensional cross sections are easier than 3D perspective views (for most)

B-*B* cross section



Process Flow in Cross Sections

* Process (simplified)

  0. Clean wafer in nasty acids (HF, HNO_3, H_2SO_4, ...)

  1. Grow 0.5 μm of SiO_2 by putting the wafer in a furnace at 1000 ^oC with O_2

  (pattern transfer subroutine)

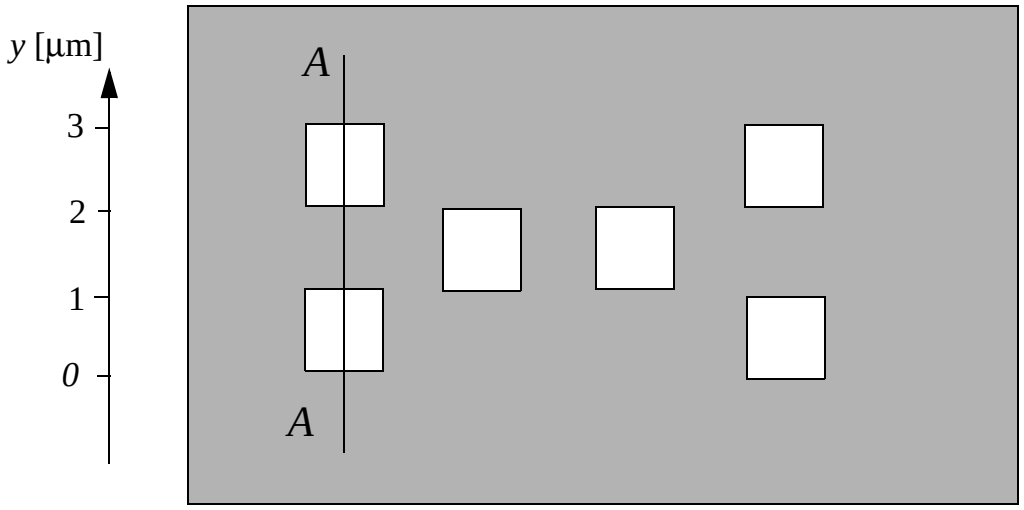
  P1. Coat the wafer with 1 μm of photoresist

  P2. Expose and develop the image and bake the resist to get rid solvent and to make it tougher

  P3. Put wafer in a plasma etcher: fluorine ions in plasma etch SiO_2 without significant etching of photoresist or silicon

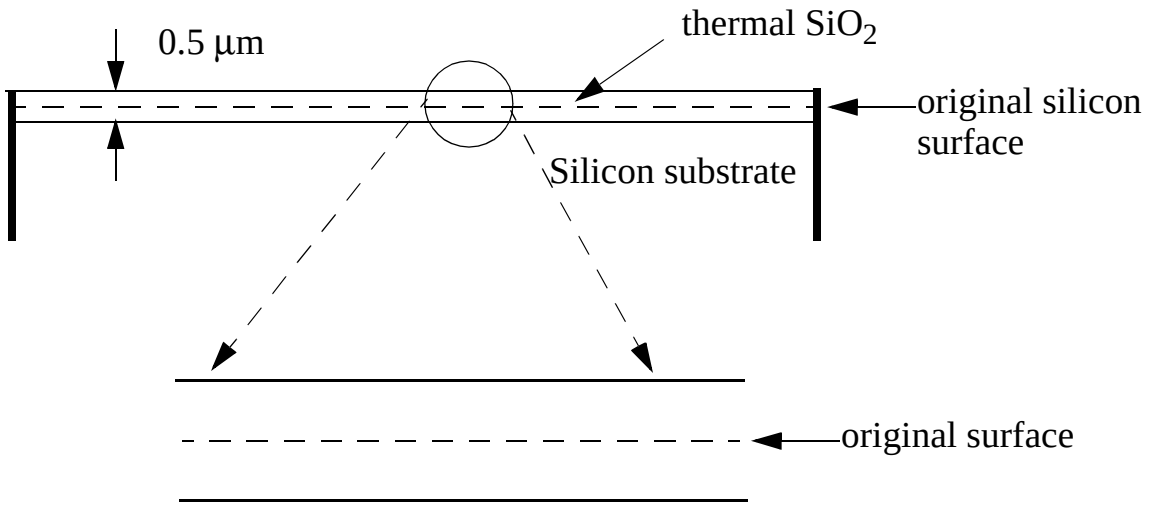
  P4. Put wafer in a plasma stripper: oxygen ions remove photoresist and leave SiO_2 untouched.

* Mask Pattern

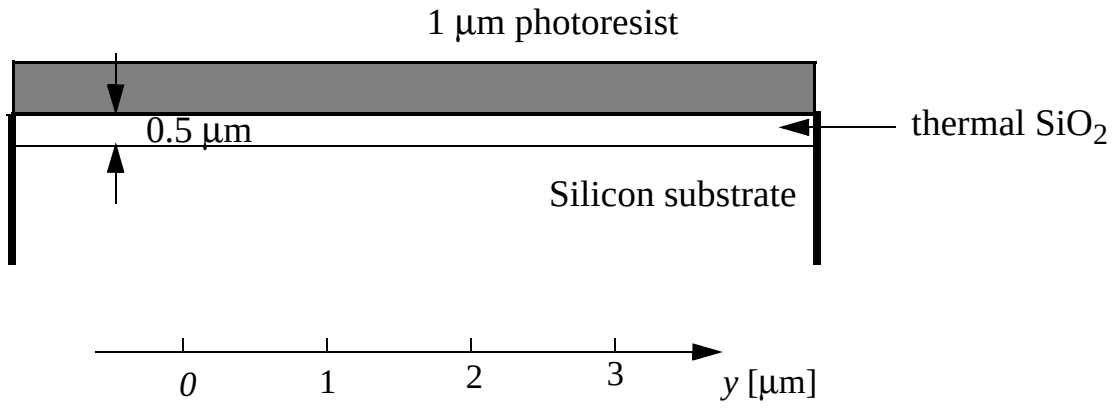


Process Flow in Cross Sections

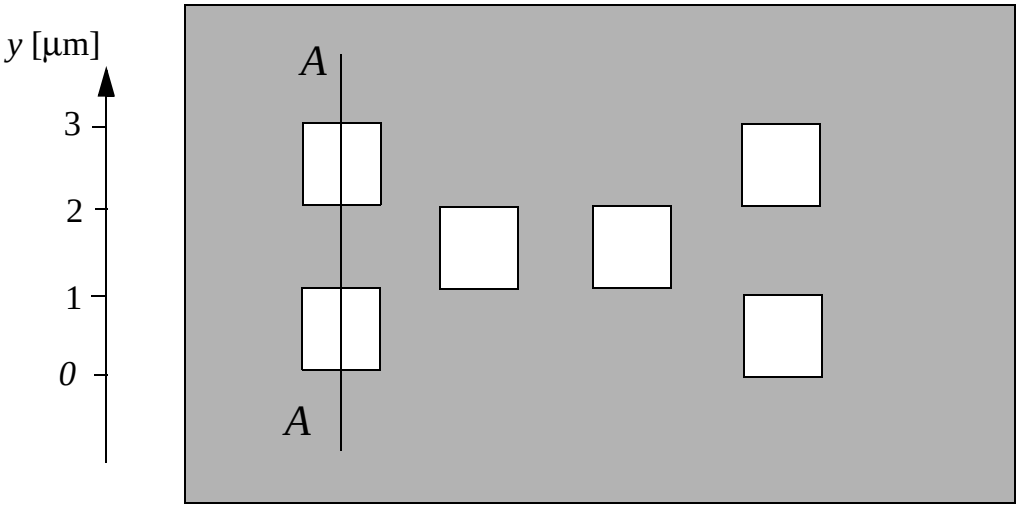
* After Step 1 (SiO_2 growth):

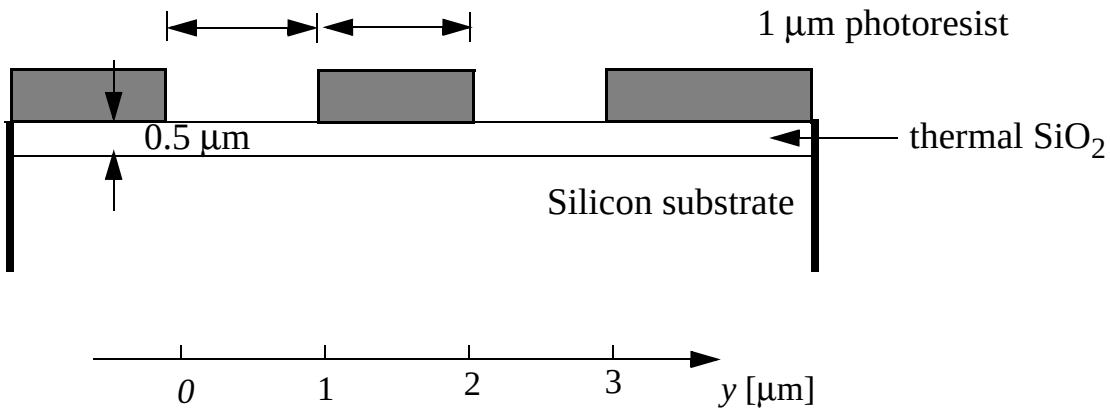


Process Cross Sections (cont.)



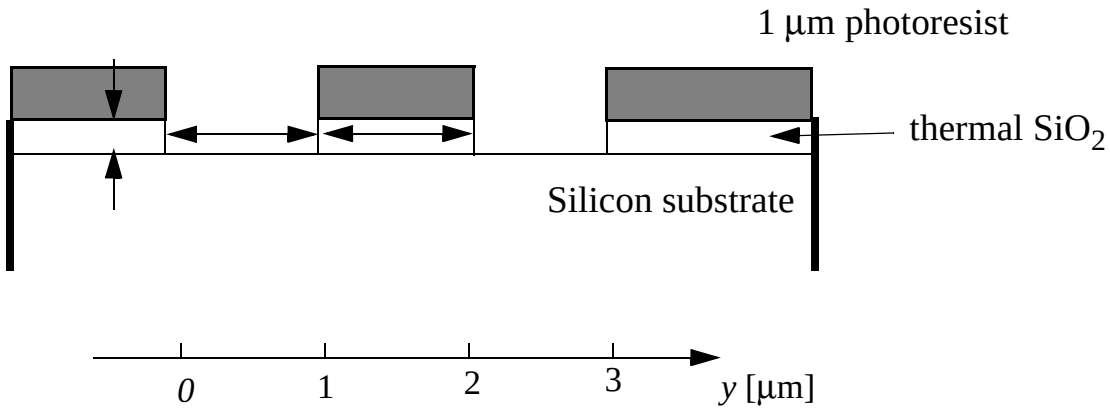
* After Step P2: photoresist has been developed from regions exposed to UV through the image of the clear areas of the mask



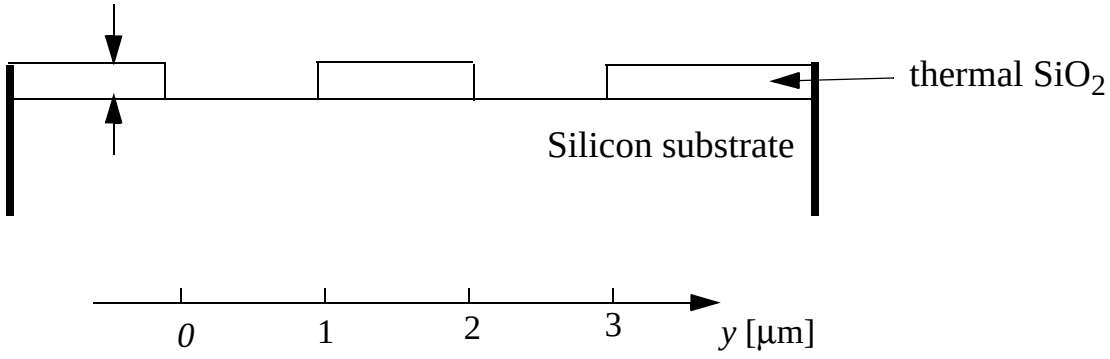

1 μm photoresist
0.5 μm
thermal SiO_2
Silicon substrate
0
1
2
3
y [μm]

Process Cross Sections (cont.)

* Cross section after step P3 (oxide etching in fluorine plasma)



* Cross section after step P4 (resist stripping)



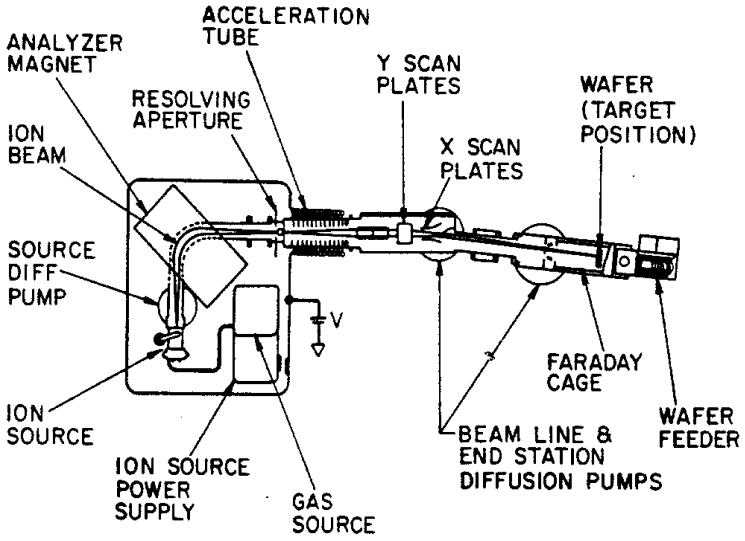
IC Processes: Ion Implantation

* How to introduce dopants into silicon?

  1. wafers are purchased from the vendor with specified substrate doping

  2. ion implantation: most common way to add dopants to the surface of wafer

* Ion implanter



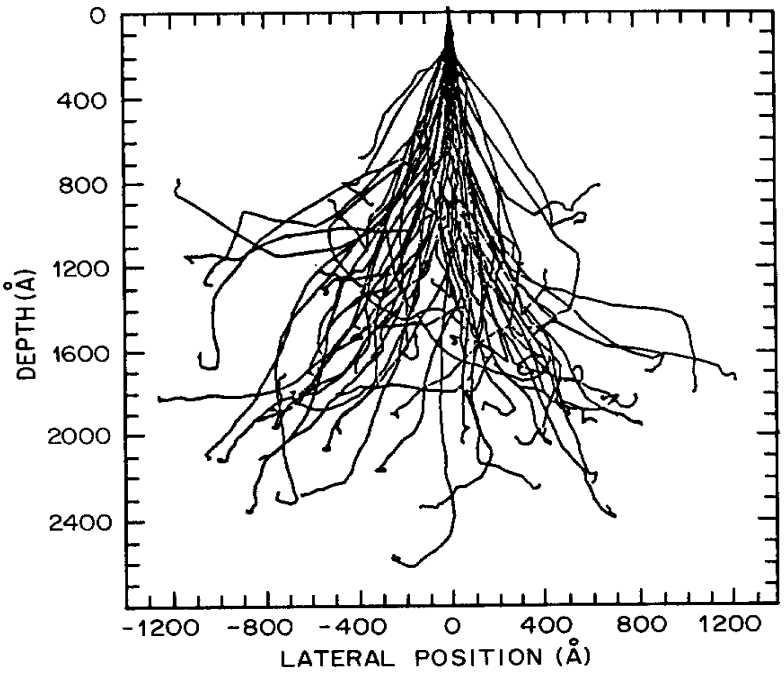
ions are generated, accelerated, and impact the wafer in a collimated beam

the beam is raster-scanned over the wafer (like the electron beam in a CRT)

energies range from 10 keV to several MeV ... range of ions in silicon is up to around 1 μm (max)

Ion Tracks in Silicon

* Each ion makes a series of collisions as it is stopped by the silicon crystal -- silicon atoms are knocked out of their positions



from: S. M. Sze, *VLSI Technology*, 2nd ed., Wiley, 1989.

* ion tracks (simulated) show that the ion density (cm^{-3}) as a function of depth is a probability distribution

* crystal order is destroyed by the implantation damage, *but*

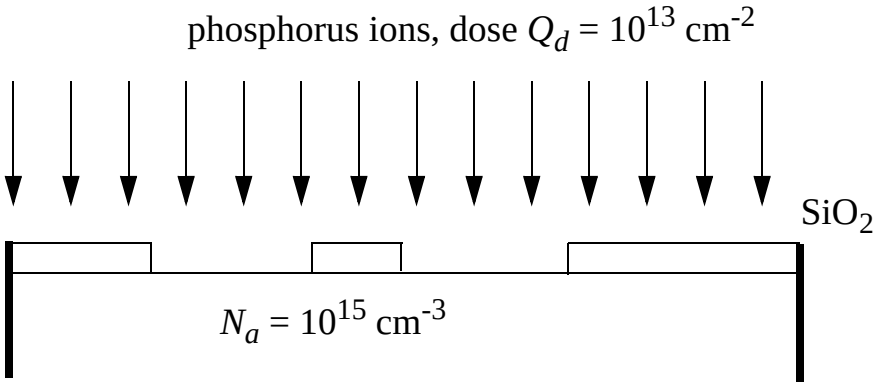
  this *amorphous* layer can be recrystallized by heating the wafer above 900 ^{o}C and most of the ions end up on lattice sites and function as donors and acceptors

  the process of repairing the damage by heating the wafer is called *annealing*

Patterned Doping by Ion Implantation

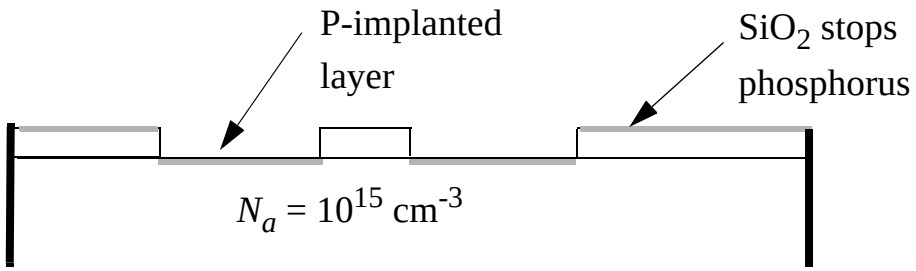
* *Dose* = ion beam flux (number cm^{-2} s^{-1}) x time for implant ... units cm^{-2}

Example:



SiO_2 film masks the implant by preventing ions from reaching the underlying silicon (assuming it's thick enough)

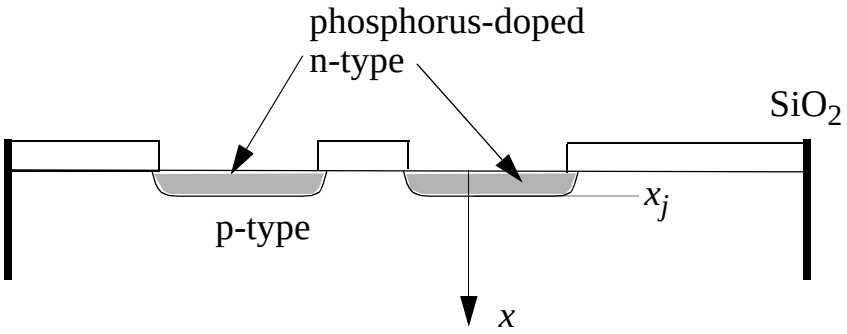
> after implantation, the phosphorus ions are confined to a damaged region near the silicon surface :



> Note: the P in the SiO_2 doesn't change its properties significantly

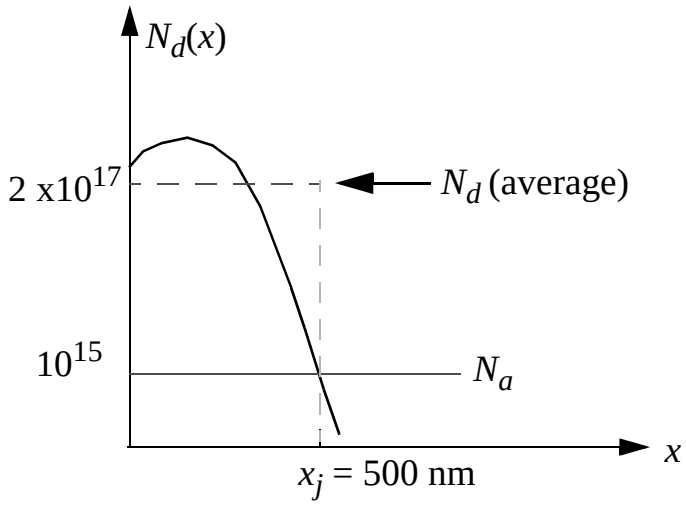
Patterned Doping by Ion Implantation (cont.)

* Annealing heals damage and also redistributes the ions (they spread farther into the silicon crystal, depending how long and how high the annealing temperature)



x_j is the *junction depth* and is the point where $N_d = N_a$

* Details of $N_d(x)$: see EE 143. We will use the average concentration in the n-type region for a given junction depth in EE 105.



* Average donor concentration in n-type layer $N_d = Q_d / x_j$

IC Materials and Processes

* *Polycrystalline silicon (polysilicon)*:

  1. silicon deposited from a gas at around 600 ^{o}C, usually with dopants added during the deposition process

  2. not a single crystal, but made up of small crystallites (grains)

  3. mobilities for holes and electrons are reduced because of the effects of the boundaries between grains

  4. used in transistors and for very short “wires” or interconnects

* *Deposited oxides*:

  1. silicon dioxide *deposited* from a gas at temperatures from 425 ^{o}C to 600 ^{o}C

  2. these oxides are known as “CVD” oxides for “chemical vapor deposition”

  3. electrical properties are inferior to thermally grown oxides

  4. used as an insulating layer between polysilicon and metal layers

* *Metals*:

  1. aluminum is the standard “wire” for ICs, but copper is beginning to be used

  2. thin layers of special metals (Ti, W) to prevent Al from reacting with silicon

IC Process

In order to make an IC, we need

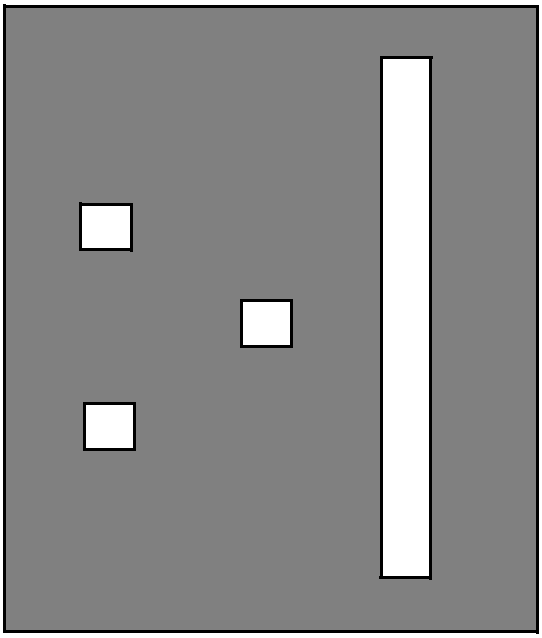
1. the mask patterns (up to 30)
2. the sequence of fabrication steps (the *process* ... or *recipe*) (up to 500)

Problem:

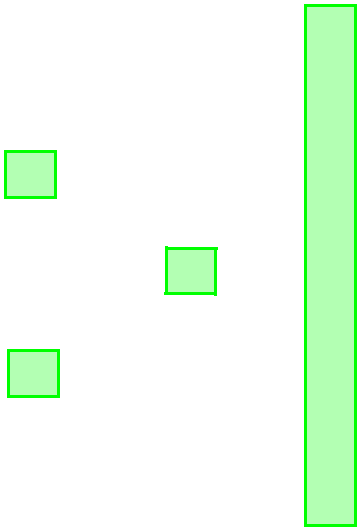
Designing the mask patterns for the IC structures using CAD requires being able to see the overlaps between patterns for several masks at once

What happens when a mask is almost all black?

mask pattern on glass plate

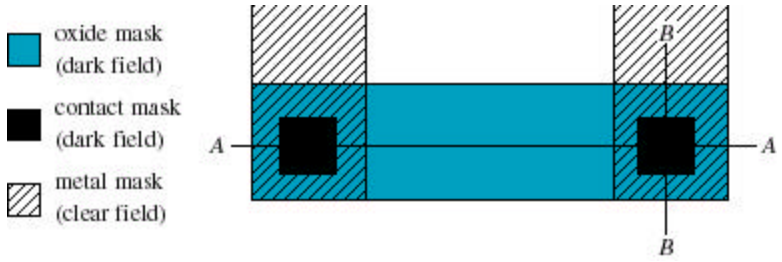


CAD layout: “draw the holes”



Process Flow Example

* Three-mask layout:



* Process (highly simplified):

1. Grow 500 nm of thermal oxide and **pattern using oxide mask**

2. Implant phosphorus and anneal

3. Deposit 600 nm of CVD oxide and **pattern using contact mask**

4. Sputter 1 μm of aluminum and **pattern using metal mask**

** note that "**pattern using xxx mask"** involves photolithography (including alignment to earlier patterns on the wafer), as well as etching using a plasma or "wet" chemicals, and finally, stripping photoresist and cleaning the wafer.

Cross Sections *A* - *A*

* Shown on layout; only draw top few μm of the silicon wafer
* Technique: keep track of dark/light field label for each mask and be careful to be consistent on what is added or etched in each step

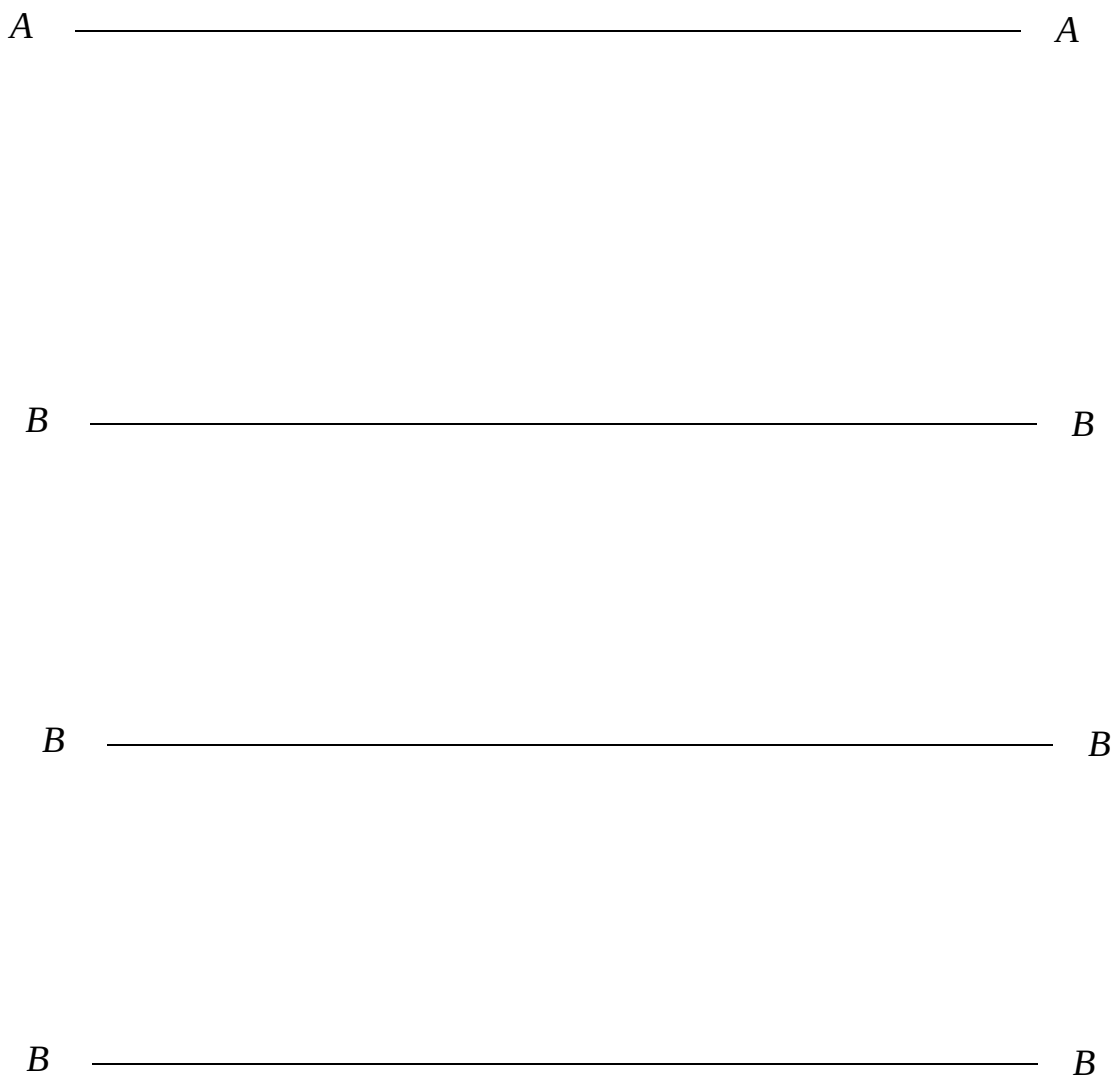
A —— *A*

A —— *A*

A —— *A*

Cross Sections *A* - *A* and *B* - *B*

* Different cross section at Al-silicon contact



n-Type Silicon Resistors

* Current is current density times cross sectional area: $A = t \times W$

$$I = \sigma_n \left(\frac{V}{L}\right) A = \left(\frac{\sigma_n A}{L}\right) V$$

Thus, the resistance of the Si resistor is given by

$R =$ $= \rho_n \frac{L}{A}$ (the familiar resistor equation)

where ρ_n is the resistivity [units: Ω-cm]

* *Silicon resistivities*:

500 Ω-cm to 5 mΩ-cm for doping concentrations from 10^{13} to 10^{19}cm^{-3}

Thus,

$R =$ $\equiv R_{sq} \cdot \frac{L}{W}$

Sheet Resistance

$$R = R_{sq}(L/W)$$

The sheet resistance is under the control of the *process designer*;

The number of squares is determined by the layout and is specified by the *IC designer*.

Example:

For average doping levels of 10^{15} cm^{-3} to 10^{19} cm^{-3} and a typical layer thickness of 0.5 μm, the sheet resistance ranges from 100 kΩ/sq to 10 Ω/sq.

Typical sheet resistances:

	Ω / square
implanted layers in Si	10 to 10^5
n^+ polysilicon (t =500 nm)	20
aluminum (t = 1 μm)	0.07
silicided polysilicon	5
silicided source/drain diffusion	3

Uncertainties in IC Fabrication

The precision of transistors and passive components fabricated using IC technology is surprisingly, *poor*!

Sources of variations:

* ion implant dose varies from point to point over the wafer and from wafer to wafer

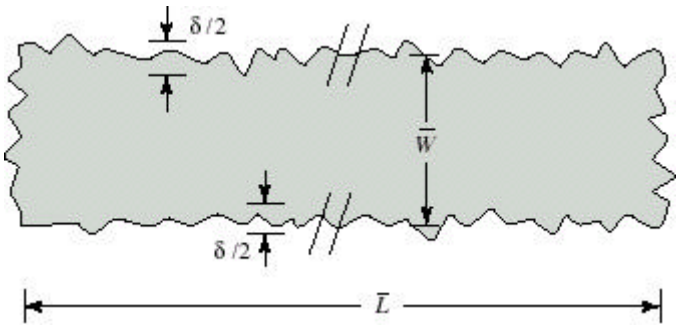
* thicknesses of layers after annealing vary due to temperature variations across the wafer

* widths of regions vary systematically due to imperfect wafer flatness (leading to focus problems) and randomly due to raggedness in the photoresist edges after development

* etc., etc.

Linewidth Uncertainties

* Due to lithographic and etching variation, the edges of a rectangle are "ragged"—greatly exaggerated in the figure



* The width is

$$W = \overline{W} \pm \frac{\delta}{2} \pm \frac{\delta}{2} = \overline{W} \pm \delta \quad \text{---->} \quad W = \overline{W}\left(1 \pm \frac{\delta}{\overline{W}}\right) = \overline{W}(1 \pm \varepsilon_W)$$

* Conclusion 1: *wider* resistors have smaller normalized uncertainty (since δ is independent of width)
* Conclusion 2: the length $L >> W$ and so its normalized uncertainty is negligible compared to that of W

Statistical Variations & Worst-Case Design

Example: IC Resistor Uncertainty

$$R = \left(\frac{1}{qN_d\mu_n t}\right)\left(\frac{L}{W}\right)$$

Note that N_d, μ_n, t, L, and W are *all* subject to variations. We can define the range for each variable in terms of a normalized uncertainty ε.

For example, $N_d = \bar{N}_d(1 \pm \varepsilon_{N_d})$ $\quad$ $L = \bar{L}(1 \pm \varepsilon_L)$, etc.

Note: how is ε defined?

assume variables are independent

typically are concerned with a multiple of the standard deviation, e.g., 6σ

RMS Uncertainties

If the variables are *independent* (meaning that there is no correlation between them), then we can count their contributions to the overall uncertainty by the "root mean square" (RMS) variation:

$$R = \left(\frac{1}{qN_d\mu_n t}\right)\left(\frac{L}{W}\right)$$

$$R = \bar{R}(1 \pm \varepsilon_R) \ .$$

The "sum of squares" of the normalized uncertainties in N_d, μ_n, t, L, and W

$$\varepsilon_R = \sqrt{\varepsilon_{N_d}^2 + \varepsilon_{\mu_n}^2 + \varepsilon_t^2 + \varepsilon_L^2 + \varepsilon_W^2}$$

The average resistance is found by substituting the averages:

$$\bar{R} = \left(\frac{1}{q\overline{N_d}\,\overline{\mu_n}\,\bar{t}}\right)\left(\frac{\bar{L}}{\bar{W}}\right)$$

Assumptions: uncertainties are << 1

Worst-Case Uncertainties

The actual situation can often be worse -- find the maximum resistance

$$R_{max} = \left(\frac{1}{qN_{d_{min}}\mu_{n_{min}}t_{min}}\right)\left(\frac{L_{max}}{W_{min}}\right)$$

Substitute in terms of individual uncertainties:

$$R_{max} = \left(\frac{1}{q\overline{N_d}(1-\varepsilon_{N_d})\bar{\mu}_n(1-\varepsilon_{\mu_n})\bar{t}(1-\varepsilon_t)}\right)\left(\frac{\bar{L}(1+\varepsilon_L)}{\bar{W}(1-\varepsilon_W)}\right)$$

Maximum resistance:

$$R_{max} \cong \bar{R}(1+\varepsilon_{N_d}+\varepsilon_{\mu_n}+\varepsilon_t+\varepsilon_L+\varepsilon_W).$$

(recall that $(1 \pm x)^{-1} \cong 1 \mp x$ for $x \ll 1$)

Minimum resistance:

$$R_{min} = \left(\frac{1}{q\overline{N_d}(1+\varepsilon_{N_d})\bar{\mu}_n(1+\varepsilon_{\mu_n})\bar{t}(1+\varepsilon_t)}\right)\left(\frac{\bar{L}(1-\varepsilon_L)}{\bar{W}(1+\varepsilon_W)}\right)$$

$$R_{min} \cong \bar{R}(1-\varepsilon_{N_d}-\varepsilon_{\mu_n}-\varepsilon_t-\varepsilon_L-\varepsilon_W)$$

Worst-Case Uncertainties (Cont.)

Maximum and minimum resistances can be written as:

$$R \cong \bar{R}(1 \pm \varepsilon_R) \qquad \varepsilon_R = \varepsilon_{N_d} + \varepsilon_{\mu_n} + \varepsilon_t + \varepsilon_L + \varepsilon_W \text{ (worst-case)}$$

Example of the difference between RMS and worst-case:

$$\varepsilon_{N_d} = 0.025 \qquad \varepsilon_{\mu_n} = 0.01 \qquad \varepsilon_t = 0.015 \qquad \varepsilon_L = 10^{-5} \qquad \varepsilon_W = 0.03$$

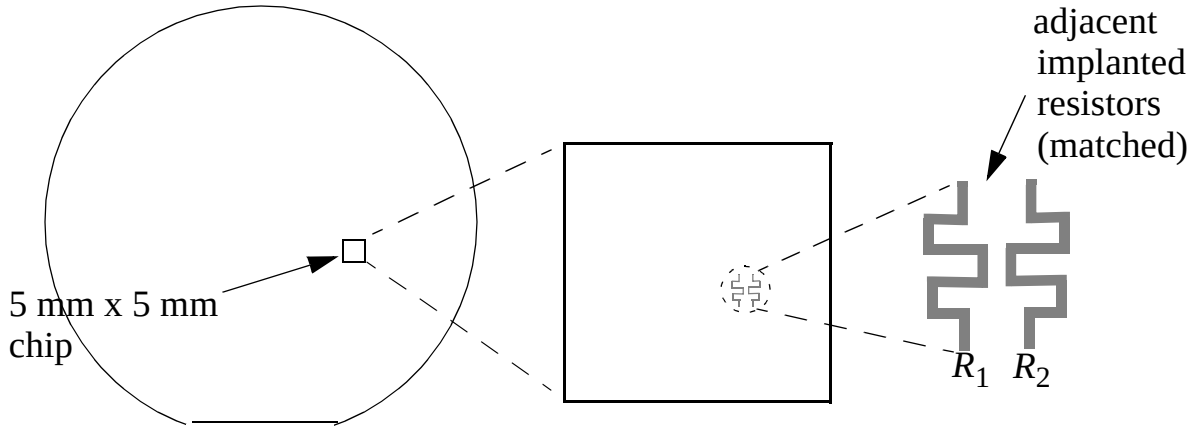
$$\varepsilon_R = \sqrt{(0.025)^2 + (0.01)^2 + (0.015)^2 + (10^{-5})^2 + (0.03)^2} = 0.043 \text{ (RMS)}$$

$$\varepsilon_R = 0.025 + 0.01 + 0.015 + 10^{-5} + 0.03 = 0.08 \text{ (worst-case)}$$

Real situation: some variables are correlated, so the answer is in between RMS and worst-case estimates

Matching of Nearby IC Resistors

* Important consideration in IC design



* Each resistor's absolute value is subject to the uncertainties in doping, mobility, and physical dimensions

Example:

R_1 and R_2 each have an average value of 10 kΩ, with a normalized uncertainty of 2% (across the wafer) and 5% (across the batch) and 10% (over a month)

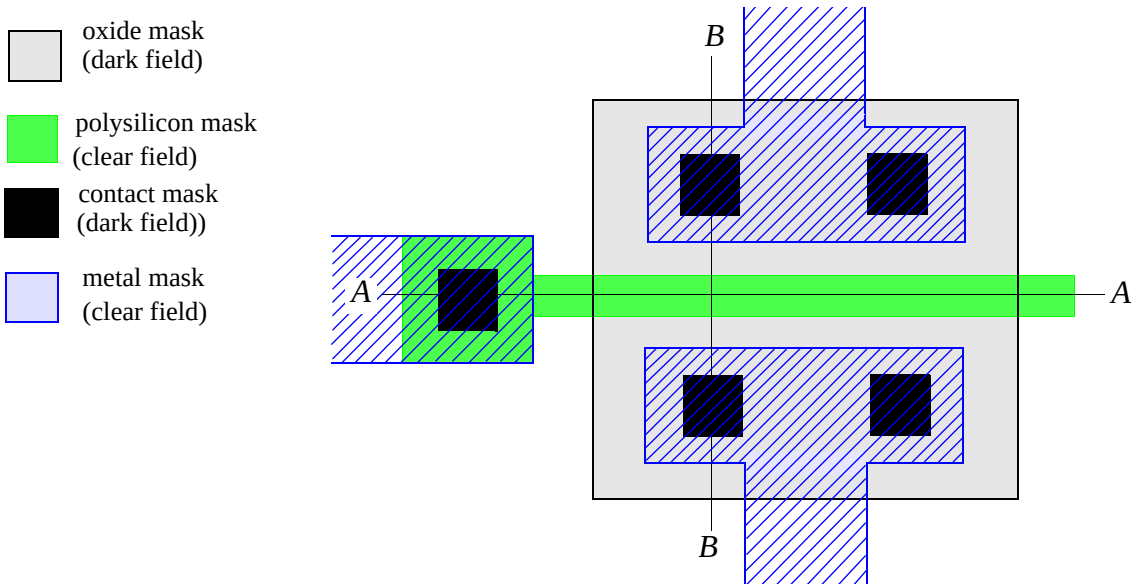
However, both resistors vary *together* ... the normalized difference is small

$$\frac{\Delta R}{\bar{R}} = \frac{|R_1 - R_2|}{(R_1 + R_2)/2} \ll \varepsilon_R \text{ (can be 0.1\% or better)}$$

MOSFET Fabrication

* This device, the subject of Chapter 4, has made possible the revolution in digital electronics. It can be made in only 4 masking steps (one of its advantages)

* Layout



Process Flow (Simplified)

1. Grow 500 nm of thermal SiO_2 and pattern using oxide mask

2. Grow 15 nm of thermal SiO_2

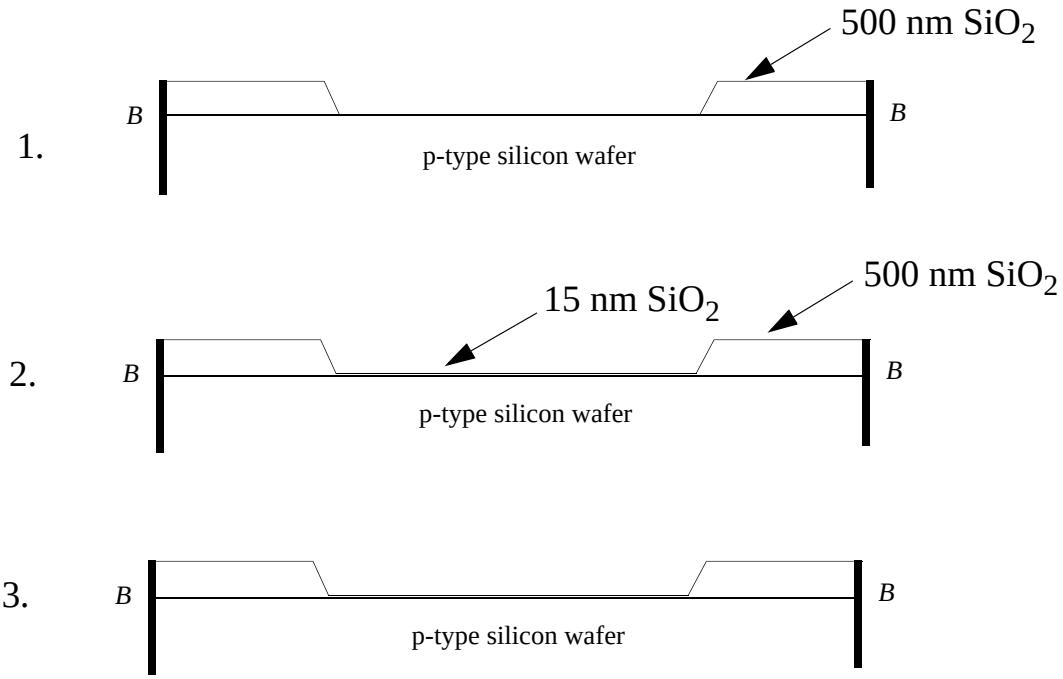
3. Deposit 500 nm of CVD polysilicon and pattern using polysilicon mask

4. Implant arsenic and anneal

5. Deposit 600 nm of CVD SiO_2 and pattern using contact mask

6. Sputter 1 μm of aluminum and pattern using metal mask.

* Cross sections along *B-B*



MOSFET Cross Sections

* Arsenic implant/anneal, CVD oxide, and metallization steps: (incomplete)

4.

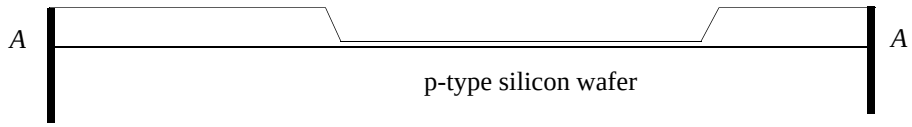
5.

6.

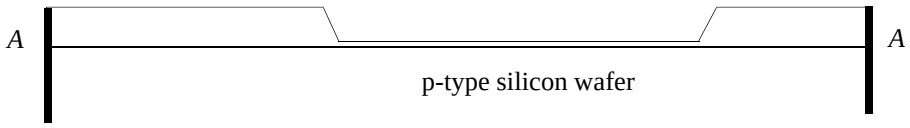
MOSFET Cross Sections (Cont.)

* Arsenic implant/anneal, CVD oxide, and metallization steps: (incomplete)

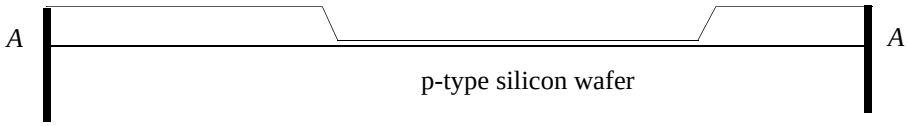
3.



5.

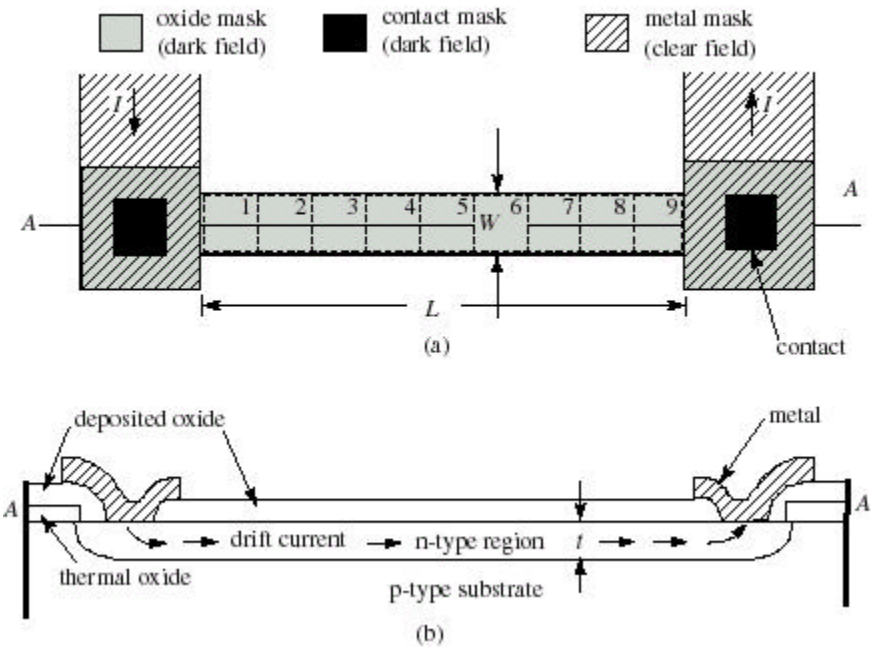


6.



IC Resistor Design

* Fabricate an n-type resistor in a p-type substrate using the process described in Chapter 2.



* The number of squares for this layout $L/W \cong 9$ squares
* To find R_{sq}:

R_{sq} =

Laying Out a Resistor

* Rough approach:

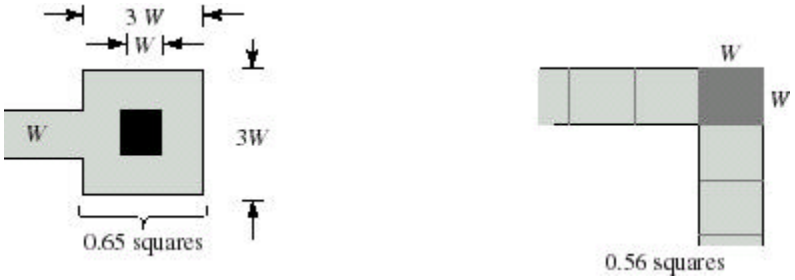
  1. R is specified, so calculate $N_{sq} = R / R_{sq}$.

  2. select a width W (possibly the minimum to save area, or to meet a requirement on the normalized uncertainty ε_W)

  3. find the length $L = W N_{sq}$ and make a rectangle L x W in area

  Add contact regions at the ends ... initially ignore their contribution to R

* More careful approach:
  account for the contact regions and also, for corners



Calculations show that the effective number of squares of the "dogbone" style contact region is 0.65 and for a 90^o corner is 0.56.

For the resistor with $L / W = 9$, the contact regions add a significant amount to the total square count:

$N_{sq} = 9 + 2\ (0.65) = 10.3$

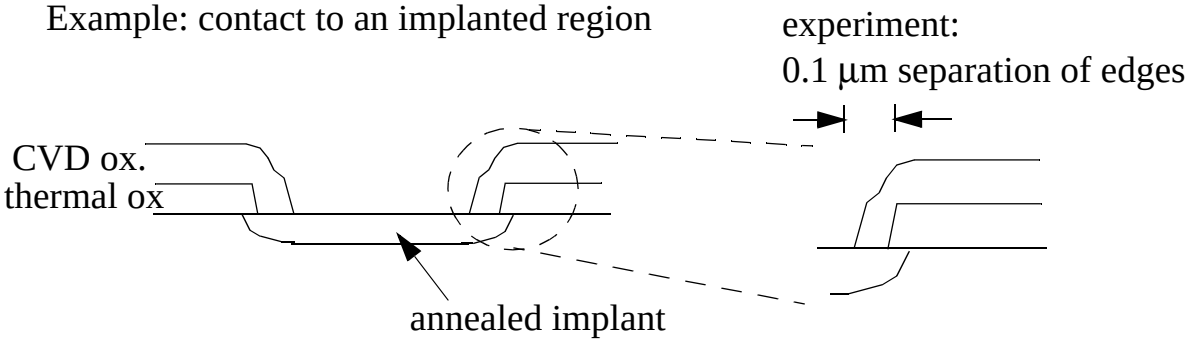
Geometric Design Rules

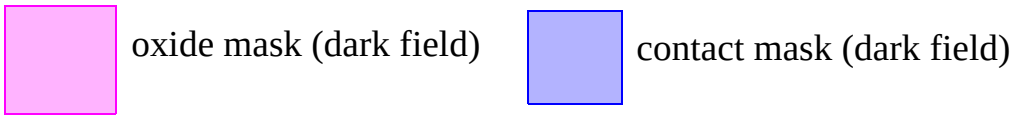
Millions of device structures must function *very reliably*, despite

1. variations in the dimensions and imperfect overlay of successive masks, and
2. and variations in the photolithography and pattern transfer process.

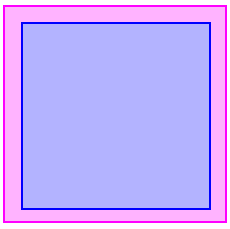
Together, these variations determine the rules for laying out masks

Example: contact to an implanted region





0.1 μm ... OK if alignment, lithography, pattern transfer is PERFECT!

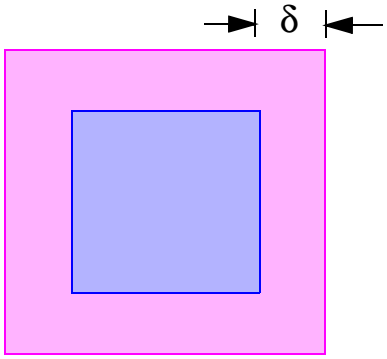


Geometric Design Rules (cont.)

* Sources of errors: *many!*

  Misalignment of masks (due to mask imperfection or stepper error or ...)

  Pattern growth/shrinkage (due to mask imperfection, exposure/development error, lateral etching under the photoresist, or ...)



overlap between masks is increased to account for error sources

  Simple approach:

  δ = physical requirement + misalignment + dimensional error

  For a 20 mask process, there are *many* interactions between masks!

How to avoid violating the design rules?

  Answer: build them into the layout CAD tool so that they can be checked automatically.

Example Design Rules for a Basic CMOS Process

Minimum dimensions specified, as well as overlaps and separations

Note that this “1 μm” process has 5μm wide wells, at the minimum, for physical reasons.