RISC-V "V" Vector Extension

Version 0.10 (also 1.0-draft-20210129)
Changes from v0.9

SLEN=VLEN layout mandatory
Support ELEN > VLEN for LMUL > 1
Defined vector FP exception behavior
Defined interaction of misa.v and mstatus.vs
Defined integer narrowing pseudo-instruction vncvt.x.x.w vd,vs,vm
Added reciprocal and reciprocal square-root estimate instructions
Added EEW encoding to whole register moves and load/stores to support microarchitectures with internal data rearrangement.

Added vrgatherei16 instruction

Rearranged bits in vtype to make vlmul bits into a contiguous field
Moved EDIV to appendix and removed instruction encoding for dot instructions to make clear not part of v1.0
Moved quad-widening mulacc to appendix and removed instruction encodings to make clear not part of v1.0
Added vneg and vfneg pseudo-instructions.

Changed mandatory illegal instruction exceptions on unsupported encodings to reserved, to allow future use of these encodings. Implementations are still recommended to trap on unsupported reserved encodings.

Clarified that support for vector misaligned memory accesses is independent of support for scalar misaligned memory accesses.

Clarified support for precise/imprecise traps. Require vstart to report location of faulting element.

Define whole register move instructions in terms of SEW instead of EEW=8 to allow definition to apply to machines with no support for EEW=8, and to help describe how these provide a hint to implementations with internal rearrangement of data. Functionality has not changed.

Specified minimum VLEN=128 for the base "V" vector extension.

Clarified whole register moves, including existence of register group save/restore, and allowed misaligned to be signaled for smallest supported size instead of encoded EEW to support implementations without SEW=8 load/store.

Changed default for vector memory instructions to be "unordered", and added ordered/unordered vector indexed instructions.

Clarified that for precise traps, vector store instructions can update idempotent memory for elements past the location of an element raising a trap.

Reserved vstart values greater than maximum element index.

Allow vector strided instruction to perform fewer memory accesses when rs2=x0.

Clarified that vsetvl{i}. x0, x0, ... form instructions may set vill when new SEW/LMUL ratio would change VLMAX.

Made clear that implementations must support LMUL 1, 2, 4, 8.

Clarified that permutation instructions also obey tail/mask agnostic/undisturbed where appropriate.

Specified that reduction instructions also obey tail agnostic/undisturbed for destination vector register for elements past first.

Mask register tail elements are always updated according to a tail-agnostic policy, regardless of vta setting.

Added mask register load/store instructions vle1, v/vse1, v to provide hint that values are masks and to reduce v1 manipulation around mask spill/fill code.

Added vsetivli instruction with immediate AVL value.

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Changes from v0.9

SLEN=VLEN layout mandatory

The group has decided to make the SLEN=VLEN layout mandatory. In-register layout of the bytes of a vector matches in-memory layout of bytes in a vector. Many of the optimizations possible with the earlier SLEN<VLEN layouts can be achieved with microarchitectural techniques on wide datapath machines, and SLEN=VLEN provides a much simpler specification and interface to software.

Support ELEN > VLEN for LMUL > 1

Specification was loosened to allow elements wider than a single vector register to be supported using a vector register group, but profiles can still mandate a minimum ELEN when LMUL = 1.

Defined vector FP exception behavior

Defined interaction of misa.v and mstatus.vs

Defined integer narrowing pseudo-instruction vncvt.x.x.w vd,vs,vm

Added reciprocal and reciprocal square-root estimate instructions

Added EEW encoding to whole register moves and load/stores to support microarchitectures with internal data rearrangement.

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Define whole register move instructions in terms of SEW instead of EEW=8 to allow definition to apply to machines with no support for EEW=8, and to help describe how these provide a hint to implementations with internal rearrangement of data. Functionality has not changed.

Specified minimum VLEN=128 for the base "V" vector extension.

Clarified whole register moves, including existence of register group save/restore, and allowed misaligned to be signaled for smallest supported size instead of encoded EEW to support implementations without
SEW=8 load/store.

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Clarified that for precise traps, vector store instructions can update idempotent memory for elements past the location of an element raising a trap.

Reserved vstart values greater than maximum element index.

Allow vector strided instruction to perform fewer memory accesses when rs2=x0.

Clarified that vsetvl{i} x0, x0, ... form instructions may set vil1 when new SEW/LMUL ratio would change VLMAX.

Made clear that implementations must support LMUL 1,2,4,8.

Clarified that permutation instructions also obey tail/mask agnostic/undisturbed where appropriate.

Specified that reduction instructions also obey tail agnostic/undisturbed for destination vector register for elements past first.

Mask register tail elements are always updated according to a tail-agnostic policy, regardless of vta setting.

Added mask register load/store instructions vle1.v/vse1.v, to provide hint that values are masks and to reduce v1 manipulation around mask spill/fill code.

Added vsetivli instruction with immediate AVL value.
1. Introduction

This document describes the draft of version 1.0 of the RISC-V vector extension.

This is a draft of the stable proposal for the vector extension specification to be used for implementation and evaluation. Once the draft label is removed, version 1.0 is intended to be sent out for public review as part of the RISC-V International ratification process. Version 1.0 is also considered stable enough to begin developing toolchains, functional simulators, and initial implementations, including in upstream software projects, and is not expected to have major functionality changes except if serious issues are discovered during ratification. Once ratified, the spec will be given version 2.0.

This draft spec is intended to capture how the complete set of currently defined vector instructions, but is not intended to determine what set of vector instructions and which supported element widths are mandatory for a given platform profile.

The term *base vector extension* is used informally to describe the standard set of vector ISA components that will be required for the single-letter "V" extension, which is intended for use in standard server and application-processor platform profiles. The set of mandatory instructions and supported element widths will vary with the base ISA (RV32I, RV64I) as described below.

Other profiles, including embedded profiles, may choose to mandate only subsets of these extensions. The exact set of mandatory supported instructions for an implementation to be compliant with a given profile will only be determined when each profile spec is ratified. For convenience in defining subset profiles, vector instruction subsets are given ISA string names beginning with the "Zv" prefix.

The document describes all the individual features to be included in the base vector extension.

The set of instructions to be included or not in the base "V" extension, and the naming of all the vector instruction subsets and extensions is still under review in this draft.

The base vector extension is designed to act as a base for additional vector extensions in various domains, including cryptography and machine learning.
2. Implementation-defined Constant Parameters

Each hart supporting the vector extension defines two parameters:

1. The maximum size of a vector element that any operation can produce or consume in bits, \( ELEN \geq 8 \), which must be a power of 2.

2. The number of bits in a single vector register, \( VLEN \), which must be a power of 2.

Profiles may set further constraints on these parameters, for example, requiring that \( ELEN \geq \max(XLEN,FLEN) \), or requiring a minimum \( VLEN \) value.

The base "V" vector extension requires that \( VLEN \geq 128 \).

The value of 128 was chosen as a compromise for application processors. Providing a larger \( VLEN \) allows stripmining code to be elided in some cases for short vectors, but also increases the size of the minimum implementation. Note that larger \( LMUL \) can be used to avoid stripmining for longer known-size application vectors at the cost of having fewer available vector register groups. For example, an \( LMUL \) of 8 allows vectors of up to sixteen 64-bit elements to be processed without stripmining using four vector register groups.

The ISA supports writing binary code that under certain constraints will execute portably on harts with different values for the \( VLEN \) parameter, provided both support the required element types.

Code can be written that will expose differences in implementation parameters.

In general, thread contexts with active vector state cannot be migrated during execution between harts that have any difference in \( VLEN \) or \( ELEN \) parameters.
### 3. Vector Extension Programmer’s Model

The vector extension adds 32 vector registers, and seven unprivileged CSRs (vstart, vxsat, vxrm, vcsr, vtype, vl, vlenb) to a base scalar RISC-V ISA.

<table>
<thead>
<tr>
<th>Address</th>
<th>Privilege</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x008</td>
<td>URW</td>
<td>vstart</td>
<td>Vector start position</td>
</tr>
<tr>
<td>0x009</td>
<td>URW</td>
<td>vxsat</td>
<td>Fixed-Point Saturate Flag</td>
</tr>
<tr>
<td>0x00A</td>
<td>URW</td>
<td>vxrm</td>
<td>Fixed-Point Rounding Mode</td>
</tr>
<tr>
<td>0x00F</td>
<td>URW</td>
<td>vcsr</td>
<td>Vector control and status register</td>
</tr>
<tr>
<td>0xC20</td>
<td>URO</td>
<td>vl</td>
<td>Vector length</td>
</tr>
<tr>
<td>0xC21</td>
<td>URO</td>
<td>vtype</td>
<td>Vector data type register</td>
</tr>
<tr>
<td>0xC22</td>
<td>URO</td>
<td>vlenb</td>
<td>VLEN/8 (vector register length in bytes)</td>
</tr>
</tbody>
</table>

#### 3.1. Vector Registers

The vector extension adds 32 architectural vector registers, v0-v31 to the base scalar RISC-V ISA.

Each vector register has a fixed VLEN bits of state.

**Note**

Zfnx (“F in X”) is a new ISA option under consideration where floating-point instructions take their arguments from the integer register file. The 1.0 vector extension is also compatible with Zfnx.

#### 3.2. Vector Context Status in mstatus

A vector context status field, VS, is added to mstatus[10:9] and shadowed in sstatus[10:9]. It is defined analogously to the floating-point context status field, FS.

Attempts to execute any vector instruction, or to access the vector CSRs, raise an illegal-instruction exception when the VS field is set to Off.

When the VS field is set to Initial or Clean, executing any instruction that changes vector state, including the vector CSRs, will change VS to Dirty. Implementations may also change VS field to Dirty at any time, even when there is no change in vector state.

**Note**

Accurate setting of the VS field is an optimization. Software will typically use VS to reduce context swap overhead.

Implementations may have a writable misa.v field. Analogous to the way in which the floating-point unit is handled, the mstatus.vs field may exist even if misa.v is clear.

**Note**

Allowing mstatus.vs to exist when misa.v is clear, enables vector emulation and simplifies handling of mstatus.vs in systems with writable misa.v.

#### 3.3. Vector type register, vtype

The read-only XLEN-wide vector type CSR, vtype provides the default type used to interpret the contents of the vector register file, and can only be updated by vset(i)vl(i) instructions. The vector type also determines the organization of elements in each vector register, and how multiple vector registers are grouped.

**Note**

Earlier drafts allowed the vtype register to be written using regular CSR writes. Allowing updates only via the vset(i)vl(i) instructions simplifies maintenance of the vtype register state.

In the base vector extension, the vtype register has five fields, vill, vma, vta, vsew[2:0], and vlmul[2:0].
Table 2. vtype register layout

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XLEN-1</td>
<td>vill</td>
<td>Illegal value if set</td>
</tr>
<tr>
<td>XLEN-2:8</td>
<td>Reserved (write 0)</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>vma</td>
<td>Vector mask agnostic</td>
</tr>
<tr>
<td>6</td>
<td>vta</td>
<td>Vector tail agnostic</td>
</tr>
<tr>
<td>5:3</td>
<td>vsew[2:0]</td>
<td>Selected element width (SEW) setting</td>
</tr>
<tr>
<td>2:0</td>
<td>vlmul[2:0]</td>
<td>Vector register group multiplier (LMUL) setting</td>
</tr>
</tbody>
</table>

Note: A small implementation supporting ELEN=32 requires only seven bits of state in vtype: two bits for ma and ta, two bits for vsew[1:0] and three bits for vlmul[2:0]. The illegal value represented by vill can be internally encoded using the illegal 64-bit combination in vsew[1:0] without requiring an additional storage bit to hold vill.

Note: Further standard and custom extensions to the vector base will extend these fields to support a greater variety of data types.

It is anticipated that an extended 64-bit instruction encoding would allow these fields to be specified statically in the instruction encoding.

3.3.1. Vector selected element width vsew[2:0]

The value in vsew sets the dynamic selected element width (SEW). By default, a vector register is viewed as being divided into VLEN/SEW elements.

Note: In the base vector "V" extension, only SEW up to ELEN = max(XLEN,FLEN) are required to be supported. Other profiles may impose different constraints on ELEN.

Table 3. vsew[2:0] (selected element width) encoding

<table>
<thead>
<tr>
<th>vsew[2:0]</th>
<th>SEW</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>8</td>
</tr>
<tr>
<td>0 0 1</td>
<td>16</td>
</tr>
<tr>
<td>0 1 0</td>
<td>32</td>
</tr>
<tr>
<td>0 1 1</td>
<td>64</td>
</tr>
<tr>
<td>1 0 0</td>
<td>128</td>
</tr>
<tr>
<td>1 0 1</td>
<td>256</td>
</tr>
<tr>
<td>1 1 0</td>
<td>512</td>
</tr>
<tr>
<td>1 1 1</td>
<td>1024</td>
</tr>
</tbody>
</table>

Note: While it is anticipated the larger vsew[2:0] encodings (100-111) will be used to encode larger SEW as shown in table, the encodings are formally reserved at this point.

Table 4. Example VLEN = 128 bits

<table>
<thead>
<tr>
<th>SEW</th>
<th>Elements per vector register</th>
</tr>
</thead>
<tbody>
<tr>
<td>64</td>
<td>2</td>
</tr>
<tr>
<td>32</td>
<td>4</td>
</tr>
<tr>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>8</td>
<td>16</td>
</tr>
</tbody>
</table>

The supported element width may vary with LMUL, but profiles may mandate the minimum SEW that must be supported with LMUL=1.

Note: The standard base V vector extension requires that SEW=max(XLEN,FLEN) is supported with LMUL=1.

Note: Some implementations may support larger SEWs only when bits from multiple vector registers are combined. Software that relies on large SEW should attempt to use the largest LMUL, and hence the fewest vector register groups, to increase the number of implementations on which the code will run. The vill bit in vtype should be checked after setting vtype to see if the configuration is supported, and an alternate code path should be provided if it is not. Alternatively, a profile can mandate the minimum SEW at each LMUL setting.
3.3.2. Vector Register Grouping (vlmul[2:0])

Multiple vector registers can be grouped together, so that a single vector instruction can operate on multiple vector registers. The term vector register group is used herein to refer to one or more vector registers used as a single operand to a vector instruction. Vector register groups allow double-width or larger elements to be operated on with the same vector length as selected-width elements. Vector register groups also provide greater execution efficiency for longer application vectors.

The vector length multiplier, $LMUL$, when greater than 1, represents the default number of vector registers that are combined to form a vector register group. Implementations must support LMUL integer values of 1, 2, 4, 8.

LMUL can also be a fractional value, reducing the number of bits used in a vector register. LMUL can have fractional values $1/2$, $1/4$, $1/8$. Fractional LMUL is used to increase the number of usable architectural registers when operating on mixed-width values, by not requiring that larger-width vectors occupy multiple vector registers. Instead, wider values can occupy a single vector register and narrower values can occupy a fraction of a vector register.

Implementations must support fractional LMUL settings for $LMUL \geq SEW_{LMUL1MIN}/SEW_{LMUL1MAX}$, where $SEW_{LMUL1MIN}$ is the narrowest supported SEW value at $LMUL=1$ and $SEW_{LMUL1MAX}$ is the widest supported SEW value at $LMUL=1$. An attempt to set an unsupported SEW and LMUL configuration sets the vill bit in vtype.

For a given supported fractional LMUL setting, implementations must support SEW settings between $SEW_{LMUL1MIN}$ and $LMUL*SEW_{LMUL1MAX}$, inclusive.

The use of vtype encodings with $LMUL < SEW_{LMUL1MIN}/SEW_{LMUL1MAX}$ is reserved, but implementations can set vill if they do not support these configurations.

LMUL is set by the signed vmlu field in vtype ($LMUL = 2^{vlmul[2:0]}$).

The derived value VMAX = LMUL*VLEN/SEW represents the maximum number of elements that can be operated on with a single vector instruction given the current SEW and LMUL settings as shown in the table below.

<table>
<thead>
<tr>
<th>vlmul[2:0]</th>
<th>LMUL</th>
<th>#groups</th>
<th>VMAX</th>
<th>Registers grouped with register n</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0 0</td>
<td>0 0</td>
<td>-</td>
<td>-</td>
<td>reserved</td>
</tr>
<tr>
<td>1 0 1</td>
<td>1/8</td>
<td>32</td>
<td>VLEN/SEW</td>
<td>v n (single register in group)</td>
</tr>
<tr>
<td>1 1 0</td>
<td>1/4</td>
<td>32</td>
<td>VLEN/SEW/4</td>
<td>v n (single register in group)</td>
</tr>
<tr>
<td>1 1 1</td>
<td>1/2</td>
<td>32</td>
<td>VLEN/SEW/2</td>
<td>v n (single register in group)</td>
</tr>
<tr>
<td>0 0 0</td>
<td>0 1</td>
<td>32</td>
<td>VLEN/SEW</td>
<td>v n (single register in group)</td>
</tr>
<tr>
<td>0 0 1</td>
<td>2 16</td>
<td>2*VLEN/SEW</td>
<td>v n, v n+1</td>
<td></td>
</tr>
<tr>
<td>0 1 0</td>
<td>4 8</td>
<td>4*VLEN/SEW</td>
<td>v n, ..., v n+3</td>
<td></td>
</tr>
<tr>
<td>0 1 1</td>
<td>8 4</td>
<td>8*VLEN/SEW</td>
<td>v n, ..., v n+7</td>
<td></td>
</tr>
</tbody>
</table>

When LMUL=2, the vector register group contains vector register v n and vector register v n+1, providing twice the vector length in bits. Instructions specifying an LMUL=2 vector register group with an odd-numbered vector register are reserved.

When LMUL=4, the vector register group contains four vector registers, and instructions specifying an LMUL=4 vector register group using vector register numbers that are not multiples of four are reserved.
When LMUL=8, the vector register group contains eight vector registers, and instructions specifying an LMUL=8 vector register group using register numbers that are not multiples of eight are reserved.

Mask registers are always contained in a single vector register, regardless of LMUL.

### 3.3.3. Vector Tail Agnostic and Vector Mask Agnostic vta and vma

These two bits modify the behavior of destination tail elements and destination inactive masked-off elements respectively during the execution of vector instructions. The tail and inactive sets contain element positions that are not receiving new results during a vector operation, as defined in Section [Preset, Active, Inactive, Body, and Tail Element Definitions](#).

All systems must support all four options:

<table>
<thead>
<tr>
<th>vta</th>
<th>vma</th>
<th>Tail Elements</th>
<th>Inactive Elements</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>undisturbed</td>
<td>undisturbed</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>undisturbed</td>
<td>agnostic</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>agnostic</td>
<td>undisturbed</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>agnostic</td>
<td>agnostic</td>
</tr>
</tbody>
</table>

When a set is marked undisturbed, the corresponding set of destination elements in a vector register group retain the value they previously held. Mask destination values are always treated as tail-agnostic, regardless of the setting of vta.

**Note:** Mask tails are always treated as agnostic to reduce complexity of managing mask data, which can be written at bit granularity. There appears to be little software need to support tail-undisturbed for mask register values.

When a set is marked agnostic, the corresponding set of destination elements in any vector destination operand can either retain the value they previously held, or are overwritten with 1s. Within a single vector instruction, each destination element can be either left undisturbed or overwritten with 1s, in any combination, and the pattern of undisturbed or overwritten with 1s is not required to be deterministic when the instruction is executed with the same inputs.

**Note:** The agnostic policy was added to accommodate machines with vector register renaming, and/or that have deeply temporal vector registers. With an undisturbed policy, all elements would have to be read from the old physical destination vector register to be copied into the new physical destination vector register. This causes an inefficiency when these inactive or tail values are not required for subsequent calculations.

**Note:** The intent is for software to reduce microarchitectural work by selecting agnostic when the value in the respective set does not matter. The value of all 1s instead of all 0s was chosen for the overwrite value to discourage software developers from depending on the value written.

**Note:** A simple in-order implementation can ignore the settings and simply execute all vector instructions using the undisturbed policy. The vta and vma state bits must still be provided in vtype for compatibility and to support thread migration.

**Note:** An out-of-order implementation can choose to implement tail-agnostic + mask-agnostic using tail-agnostic + mask-undisturbed to reduce implementation complexity.

**Note:** The definition of agnostic result policy is left loose to accommodate migrating application threads between harts on a small in-order core (which probably leaves agnostic regions undisturbed) and harts on a larger out-of-order core with register renaming (which probably overwrites agnostic elements with 1s). As it might be necessary to restart in the middle, we allow arbitrary mixing of agnostic policies within a single vector instruction. This allowed mixing of policies also enables implementations that might change policies for different granules of a vector register, for example, using undisturbed within a granule that is actively operated on but renaming to all 1s for granules in the tail.

The assembly syntax adds two flags to the `vsetvli` instruction:

```assembly
  ta   # Tail agnostic
  tu   # Tail undisturbed
  ma   # Mask agnostic
  mu   # Mask undisturbed

  vsetvli t0, a0, e32,m4,ta,ma  # Tail agnostic, mask agnostic
  vsetvli t0, a0, e32,m4,tu,ma  # Tail undisturbed, mask agnostic
  vsetvli t0, a0, e32,m4,ta,mu  # Tail agnostic, mask undisturbed
  vsetvli t0, a0, e32,m4,tu,mu  # Tail undisturbed, mask undisturbed
```
3.3.4. Vector Type Illegal \texttt{vill}

The \texttt{vill} bit is used to encode that a previous \texttt{vset{i}vl{i}} instruction attempted to write an unsupported value to \texttt{vtype}.

\begin{itemize}
  \item[Note] The \texttt{vill} bit is held in bit XLEN-1 of the CSR to support checking for illegal values with a branch on the sign bit.
  \item[Note] If the \texttt{vill} bit is set, then any attempt to execute a vector instruction that depends upon \texttt{vtype} will raise an illegal-instruction exception.
  \item[Note] \texttt{vset{i}vl{i}} and whole-register loads, stores, and moves do not depend upon \texttt{vtype}.
\end{itemize}

When the \texttt{vill} bit is set, the other XLEN-1 bits in \texttt{vtype} shall be zero.

3.4. Vector Length Register \texttt{vl}

The \texttt{XLEN}-bit-wide read-only \texttt{vl} CSR can only be updated by the \texttt{vset{i}vl{i}} instructions, and the \texttt{fault-only-first} vector load instruction variants.

The \texttt{vl} register holds an unsigned integer specifying the number of elements to be updated by a vector instruction.

\begin{itemize}
  \item[Note] The number of bits implemented in \texttt{vl} depends on the implementation’s maximum vector length of the smallest supported type. The smallest vector implementation with VLEN=32 and supporting SEW=8 would need at least six bits in \texttt{vl} to hold the values 0-32 (VLEN=32, with LMUL=8 and SEW=8, yields VLMAX=32).
  \item[Note] Elements in any destination vector register group with indices $\geq \texttt{vl}$ are unmodified during execution of a vector instruction. When $\texttt{vstart} \geq \texttt{vl}$, no elements are updated in any destination vector register group.
  \item[Note] As a consequence, when \texttt{vl}=0, no elements are updated in the destination vector register group, regardless of \texttt{vstart}.
\end{itemize}

Instructions that write an \texttt{x} register or \texttt{f} register do so even when $\texttt{vstart} \geq \texttt{vl}$.

3.5. Vector Byte Length \texttt{vlenb}

The \texttt{XLEN}-bit-wide read-only CSR \texttt{vlenb} holds the value VLEN/8, i.e., the vector register length in bytes.

\begin{itemize}
  \item[Note] The value in \texttt{vlenb} is a design-time constant in any implementation.
  \item[Note] Without this CSR, several instructions are needed to calculate VLEN in bytes, and the code has to disturb current \texttt{vl} and \texttt{vtype} settings which require them to be saved and restored.
\end{itemize}

3.6. Vector Start Index CSR \texttt{vstart}

The \texttt{vstart} read-write CSR specifies the index of the first element to be executed by a vector instruction.

Normally, \texttt{vstart} is only written by hardware on a trap on a vector instruction, with the \texttt{vstart} value representing the element on which the trap was taken (either a synchronous exception or an asynchronous interrupt), and at which execution should resume after a resumable trap is handled.

All vector instructions are defined to begin execution with the element number given in the \texttt{vstart} CSR, leaving earlier elements in the destination vector undisturbed, and to reset the \texttt{vstart} CSR to zero at the end of execution.

\begin{itemize}
  \item[Note] All vector instructions, including \texttt{vset{i}vl{i}}, reset the \texttt{vstart} CSR to zero.
\end{itemize}

\texttt{vstart} is not modified by vector instructions that raise illegal-instruction exceptions.
For instructions where the number of elements to be performed is set by \( v_1 \), if the value in the \( v_{\text{start}} \) register is greater than or equal to the vector length \( v_1 \) then no element operations are performed. The \( v_{\text{start}} \) register is then reset to zero.

The \( v_{\text{start}} \) CSR is defined to have only enough writable bits to hold the largest element index (one less than the maximum \( \text{VLMAX} \)).

Note: The maximum vector length is obtained with the largest LMUL setting (8) and the smallest SEW setting (8), so \( \text{VLMAX}_{\text{max}} = 8^*\text{VLEN}/8 = \text{VLEN} \). For example, for \( \text{VLEN}=256 \), \( v_{\text{start}} \) would have 8 bits to represent indices from 0 through 255.

The use of \( v_{\text{start}} \) values greater than the largest element index for the current SEW setting is reserved.

Note: It is recommended that implementations trap if \( v_{\text{start}} \) is out of bounds. It is not required to trap, as a possible future use of upper \( v_{\text{start}} \) bits is to store imprecise trap information.

The \( v_{\text{start}} \) CSR is writable by unprivileged code, but non-zero \( v_{\text{start}} \) values may cause vector instructions to run substantially slower on some implementations, so \( v_{\text{start}} \) should not be used by application programmers. A few vector instructions cannot be executed with a non-zero \( v_{\text{start}} \) value and will raise an illegal instruction exception as defined below.

Note: Making \( v_{\text{start}} \) visible to unprivileged code supports user-level threading libraries.

Implementations are permitted to raise illegal instruction exceptions when attempting to execute a vector instruction with a value of \( v_{\text{start}} \) that the implementation can never produce when executing that same instruction with the same \( v\text{type} \) setting.

Note: For example, some implementations will never take interrupts during execution of a vector arithmetic instruction, instead waiting until the instruction completes to take the interrupt. Such implementations are permitted to raise an illegal instruction exception when attempting to execute a vector arithmetic instruction when \( v_{\text{start}} \) is nonzero.

Note: When migrating a software thread between two harts with different microarchitectures, the \( v_{\text{start}} \) value might not be supported by the new hart microarchitecture. The runtime on the receiving hart might then have to emulate instruction execution to a supported \( v_{\text{start}} \) element position. Alternatively, migration events can be constrained to only occur at mutually supported \( v_{\text{start}} \) locations.

3.7. Vector Fixed-Point Rounding Mode Register \( \text{vxrm} \)

The vector fixed-point rounding-mode register holds a two-bit read-write rounding-mode field. The vector fixed-point rounding-mode is given a separate CSR address to allow independent access, but is also reflected as a field in \( \text{vcsr} \).

The fixed-point rounding algorithm is specified as follows. Suppose the pre-rounding result is \( v \), and \( d \) bits of that result are to be rounded off. Then the rounded result is \((v >> d) + r\), where \( r \) depends on the rounding mode as specified in the following table.

<table>
<thead>
<tr>
<th>( \text{vxrm}[1:0] )</th>
<th>Abbreviation</th>
<th>Rounding Mode</th>
<th>Rounding increment, ( r )</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>0</td>
<td>round-to-nearest-up (add +0.5 LSB)</td>
<td>( v[d-1] )</td>
</tr>
<tr>
<td>01</td>
<td>1</td>
<td>round-to-nearest-even</td>
<td>( v[d-1] ) &amp; (( v[d-2:0])≠0</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>round-down (truncate)</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>round-to-odd (OR bits into LSB, aka &quot;jam&quot;)</td>
<td>( !v[d] ) &amp; ( v[d-1:0])≠0</td>
</tr>
</tbody>
</table>

The rounding functions:

\[
\text{roundoff}_\text{unsigned}(v, d) = (\text{unsigned}(v) \gg d) + r \\
\text{roundoff}_\text{signed}(v, d) = (\text{signed}(v) \gg d) + r
\]

are used to represent this operation in the instruction descriptions below.

\( \text{vxrm}[XLEN–1:2] \) should be written as zeros.

Note: A new rounding mode can be set while saving the original rounding mode using a single \text{csrwi} instruction.
3.8. Vector Fixed-Point Saturation Flag vxsat

The vxsat CSR holds a single read-write bit that indicates if a fixed-point instruction has had to saturate an output value to fit into a destination format.

The vxsat bit is mirrored in vcsr.

3.9. Vector Control and Status Register vcsr

The vxrm and vxsat separate CSRs can also be accessed via fields in the vector control and status CSR, vcsr.

Table 6. vcsr layout

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:1</td>
<td>vxrm[1:0]</td>
<td>Fixed-point rounding mode</td>
</tr>
<tr>
<td>0</td>
<td>vxsat</td>
<td>Fixed-point accrued saturation flag</td>
</tr>
</tbody>
</table>

3.10. State of Vector Extension at Reset

The vector extension must have a consistent state at reset. In particular, vtype and vl must have values that can be read and then restored with a single vsetvl instruction.

Note: It is recommended that at reset, vtype.vill is set, the remaining bits in vtype are zero, and vl is set to zero.

The vstart, vxrm, vxsat CSRs can have arbitrary values at reset.

Note: Any use of the vector unit will require an initial vset{i}vl{i}, which will reset vstart. The vxrm and vxsat fields should be reset explicitly in software before use.

The vector registers can have arbitrary values at reset.
4. Mapping of Vector Elements to Vector Register State

The following diagrams illustrate how different width elements are packed into the bytes of a vector register depending on the current SEW and LMUL settings, as well as implementation VLEN. Elements are packed into each vector register with the least-significant byte in the lowest-numbered bits.

4.1. Mapping for LMUL = 1

When LMUL=1, elements are simply packed in order from the least-significant to most-significant bits of the vector register.

Note: To increase readability, vector register layouts are drawn with bytes ordered from right to left with increasing byte address. Bits within an element are numbered in a little-endian format with increasing bit index from right to left corresponding to increasing magnitude.

LMUL=1 examples.

The element index is given in hexadecimal and is shown placed at the least-significant byte of the stored element.

VLEN=32b

<table>
<thead>
<tr>
<th>Byte</th>
<th>3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEW=8b</td>
<td>3 2 1 0</td>
</tr>
<tr>
<td>SEW=16b</td>
<td>1 0</td>
</tr>
<tr>
<td>SEW=32b</td>
<td>0</td>
</tr>
</tbody>
</table>

VLEN=64b

<table>
<thead>
<tr>
<th>Byte</th>
<th>7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEW=8b</td>
<td>7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>SEW=16b</td>
<td>3 2 1 0</td>
</tr>
<tr>
<td>SEW=32b</td>
<td>1 0</td>
</tr>
<tr>
<td>SEW=64b</td>
<td>0</td>
</tr>
</tbody>
</table>

VLEN=128b

<table>
<thead>
<tr>
<th>Byte</th>
<th>F E D C B A 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEW=8b</td>
<td>F E D C B A 9 8 7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>SEW=16b</td>
<td>7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>SEW=32b</td>
<td>3 2 1 0</td>
</tr>
<tr>
<td>SEW=64b</td>
<td>1 0</td>
</tr>
<tr>
<td>SEW=128b</td>
<td>0</td>
</tr>
</tbody>
</table>

VLEN=256b

<table>
<thead>
<tr>
<th>Byte</th>
<th>1F1E1D1C1B1A19181716151413121110 F E D C B A 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEW=8b</td>
<td>1F1E1D1C1B1A19181716151413121110 F E D C B A 9 8 7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>SEW=16b</td>
<td>F E D C B A 9 8 7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>SEW=32b</td>
<td>7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>SEW=64b</td>
<td>3 2 1 0</td>
</tr>
<tr>
<td>SEW=128b</td>
<td>1 0</td>
</tr>
</tbody>
</table>

4.2. Mapping for LMUL < 1

When LMUL < 1, only the first LMUL*VLEN/SEW elements in the vector register are used. The remaining space in the vector register is treated as part of the tail.
4.3. Mapping with LMUL > 1

When vector registers are grouped, the elements of the vector register group are striped across the constituent vector registers. The elements are packed contiguously in element order in each vector register in the group, moving to the next highest-numbered vector register in the group once each vector register is filled.
LMUL > 1 examples

<table>
<thead>
<tr>
<th>VLEN=32b, SEW=8b, LMUL=2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte</td>
</tr>
<tr>
<td>v2*n</td>
</tr>
<tr>
<td>v2*n+1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VLEN=32b, SEW=16b, LMUL=2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte</td>
</tr>
<tr>
<td>v2*n</td>
</tr>
<tr>
<td>v2*n+1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VLEN=32b, SEW=16b, LMUL=4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte</td>
</tr>
<tr>
<td>v4*n</td>
</tr>
<tr>
<td>v4*n+1</td>
</tr>
<tr>
<td>v4*n+2</td>
</tr>
<tr>
<td>v4*n+3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VLEN=32b, SEW=32b, LMUL=4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte</td>
</tr>
<tr>
<td>v4*n</td>
</tr>
<tr>
<td>v4*n+1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VLEN=64b, SEW=32b, LMUL=2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte</td>
</tr>
<tr>
<td>v2*n</td>
</tr>
<tr>
<td>v2*n+1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VLEN=64b, SEW=32b, LMUL=4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte</td>
</tr>
<tr>
<td>v4*n</td>
</tr>
<tr>
<td>v4*n+1</td>
</tr>
<tr>
<td>v4*n+2</td>
</tr>
<tr>
<td>v4*n+3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VLEN=128b, SEW=32b, LMUL=2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte</td>
</tr>
<tr>
<td>v2*n</td>
</tr>
<tr>
<td>v2*n+1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VLEN=128b, SEW=32b, LMUL=4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte</td>
</tr>
<tr>
<td>v4*n</td>
</tr>
<tr>
<td>v4*n+1</td>
</tr>
<tr>
<td>v4*n+2</td>
</tr>
<tr>
<td>v4*n+3</td>
</tr>
</tbody>
</table>

4.4. Mapping across Mixed-Width Operations

The vector ISA is designed to support mixed-width operations without requiring explicit additional rearrangement instructions. The recommended software strategy when operating on vectors of different precision values is to modify vtype
dynamically to keep SEW/LMUL constant (and hence VLMAX constant).

The following example shows four different packed element widths (8b, 16b, 32b, 64b) in a VLEN=128b implementation. The vector register grouping factor (LMUL) is increased by the relative element size such that each group can hold the same number of vector elements (VLMAX=8 in this example) to simplify stripmining code.

Example VLEN=128b, with SEW/LMUL=16

<table>
<thead>
<tr>
<th>Byte</th>
<th>F E D C B A 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>vn</td>
<td>- - - - - - - - 7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>vn</td>
<td>7 6 5 4 3 2 1 0 SEW=16b, LMUL=1</td>
</tr>
<tr>
<td>v2*n</td>
<td>3 2 1 0 SEW=32b, LMUL=2</td>
</tr>
<tr>
<td>v2*n+1</td>
<td>7 6 5 4</td>
</tr>
<tr>
<td>v4*n</td>
<td>1 0 SEW=64b, LMUL=4</td>
</tr>
<tr>
<td>v4*n+1</td>
<td>3 2</td>
</tr>
<tr>
<td>v4*n+2</td>
<td>5 4</td>
</tr>
<tr>
<td>v4*n+3</td>
<td>7 6</td>
</tr>
</tbody>
</table>

The following table shows each possible constant SEW/LMUL operating point for loops with mixed-width operations. Each column represents a constant SEW/LMUL operating point. Entries in table are the LMUL values that yield that column’s SEW/LMUL value for the datawidth on that row. In each column, an LMUL setting for a datawidth indicates that it can be aligned with the other datawidths in the same column that also have an LMUL setting, such that all have the same VLMAX.

| SEW/LMUL | 1 | 2 | 4 | 8 | 16 | 32 | 64 | 128 | 256 | 512 | 1024 | 2048 | 4096 | 8192 |
|----------|---|---|---|---|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| SEW=8    | 8 | 4 | 2 | 1 | 1/2 | 1/4 | 1/8 |
| SEW=16   | 8 | 4 | 2 | 1 | 1/2 | 1/4 | 1/8 |
| SEW=32   | 8 | 4 | 2 | 1 | 1/2 | 1/4 | 1/8 |
| SEW=64   | 8 | 4 | 2 | 1 | 1/2 | 1/4 | 1/8 |
| SEW=128  | 8 | 4 | 2 | 1 | 1/2 | 1/4 | 1/8 |
| SEW=256  | 8 | 4 | 2 | 1 | 1/2 | 1/4 | 1/8 |
| SEW=512  | 8 | 4 | 2 | 1 | 1/2 | 1/4 | 1/8 |
| SEW=1024 | 8 | 4 | 2 | 1 | 1/2 | 1/4 | 1/8 |

Larger LMUL settings can also be used to simply increase vector length to reduce instruction fetch and dispatch overheads in cases where fewer vector register groups are needed.

Note: The SEW/LMUL values of 2048 and greater are shown in the table for completeness but they do not add a useful operating point in the base architecture as they use less than the full register capacity and do not enable more architectural registers.

4.5. Mapping with LMUL > 1 and ELEN > VLEN

If vector registers are grouped to support larger SEW, with ELEN > VLEN, the vector registers in the group are concatenated to form a single array of bytes, with the lowest-numbered register in the group holding the lowest-addressed bytes from the memory layout.
LMUL > 1 ELEN>VLEN, examples

VLEN=32b, SEW=64b, LMUL=2

<table>
<thead>
<tr>
<th>Byte</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>v2*n</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>v2*n+1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VLEN=32b, SEW=64b, LMUL=4

<table>
<thead>
<tr>
<th>Byte</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>v4*n</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>v4*n+1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>v4*n+2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>v4*n+3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

VLEN=32b, SEW=64b, LMUL=8

<table>
<thead>
<tr>
<th>Byte</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>v8*n</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>v8*n+1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>v8*n+2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>v8*n+3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>v8*n+4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>v8*n+5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>v8*n+6</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>v8*n+7</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 4.6. Mask Register Layout

A vector mask occupies only one vector register regardless of SEW and LMUL. Each element is allocated a single mask bit in a mask vector register.

**Note:** Earlier designs (pre-0.9) had a varying number of bits per mask value (MLEN). In the 0.9 design, MLEN=1.

#### 4.6.1. Mask Element Locations

The mask bit for element *i* is located in bit *i* of the mask register, independent of SEW or LMUL.

VLEN=32b

<table>
<thead>
<tr>
<th>Byte</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMUL=1, SEW=8b</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Element</td>
<td>[03][02][01][00]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mask bit position in decimal</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

LMUL=2, SEW=16b

<table>
<thead>
<tr>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>[01]</td>
<td>[00]</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>[03]</td>
<td>[02]</td>
</tr>
</tbody>
</table>

LMUL=4, SEW=32b

<table>
<thead>
<tr>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>[00]</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>[01]</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>[02]</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>[03]</td>
</tr>
</tbody>
</table>
LMUL=2, SEW=8b

3 2 1 0
[03][02][01][00]
7 6 5 4
[07][06][05][04]

LMUL=8, SEW=32b

0
[00]
1
[01]
2
[02]
3
[03]
4
[04]
5
[05]
6
[06]
7
[07]

LMUL=8, SEW=8b

3 2 1 0
[03][02][01][00]
7 6 5 4
[07][06][05][04]
B A 9 8
[11][10][09][08]
F E D C
[15][14][13][12]
13 12 11 10
[19][18][17][16]
17 16 15 14
[23][22][21][20]
1B 1A 19 18
[27][26][25][24]
1F 1E 1D 1C
[31][30][29][28]
5. Vector Instruction Formats

The instructions in the vector extension fit under three existing major opcodes (LOAD-FP, STORE-FP, AMO) and one new major opcode (OP-V).

Vector loads and stores are encoded within the scalar floating-point load and store major opcodes (LOAD-FP/STORE-FP). The vector load and store encodings repurpose a portion of the standard scalar floating-point load/store 12-bit immediate field to provide further vector instruction encoding, with bit 25 holding the standard vector mask bit (see Mask Encoding).

Format for Vector Load Instructions under LOAD-FP major opcode

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>nf</td>
<td>31</td>
<td>Function</td>
</tr>
<tr>
<td>mew</td>
<td>29-28</td>
<td>Mode exponent width</td>
</tr>
<tr>
<td>vm</td>
<td>27-26</td>
<td>Vector mask bit</td>
</tr>
<tr>
<td>lumop</td>
<td>25</td>
<td>Load/unload mode op</td>
</tr>
<tr>
<td>rs1</td>
<td>20-14</td>
<td>Source register</td>
</tr>
<tr>
<td>width</td>
<td>13-12</td>
<td>Vector width</td>
</tr>
<tr>
<td>vd</td>
<td>7-6</td>
<td>Destination register</td>
</tr>
<tr>
<td>0</td>
<td>0-0</td>
<td>Immediate data</td>
</tr>
</tbody>
</table>

Format for Vector Store Instructions under STORE-FP major opcode

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>nf</td>
<td>31</td>
<td>Function</td>
</tr>
<tr>
<td>mew</td>
<td>29-28</td>
<td>Mode exponent width</td>
</tr>
<tr>
<td>vm</td>
<td>27-26</td>
<td>Vector mask bit</td>
</tr>
<tr>
<td>sumop</td>
<td>25</td>
<td>Store/unload mode op</td>
</tr>
<tr>
<td>rs1</td>
<td>20-14</td>
<td>Source register</td>
</tr>
<tr>
<td>width</td>
<td>13-12</td>
<td>Vector width</td>
</tr>
<tr>
<td>vs3</td>
<td>7-6</td>
<td>Destination register</td>
</tr>
<tr>
<td>0</td>
<td>0-0</td>
<td>Immediate data</td>
</tr>
</tbody>
</table>

Format for Vector AMO Instructions under AMO major opcode

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>amoop</td>
<td>31</td>
<td>Address mode op</td>
</tr>
<tr>
<td>wd</td>
<td>27-26</td>
<td>Width exponent</td>
</tr>
<tr>
<td>vm</td>
<td>25</td>
<td>Vector mask bit</td>
</tr>
<tr>
<td>vs2</td>
<td>20-14</td>
<td>Source vector register</td>
</tr>
<tr>
<td>rs1</td>
<td>13-12</td>
<td>Register</td>
</tr>
<tr>
<td>vs3</td>
<td>7-6</td>
<td>Store vector register</td>
</tr>
<tr>
<td>0</td>
<td>0-0</td>
<td>Immediate data</td>
</tr>
</tbody>
</table>

Formats for Vector Arithmetic Instructions under OP-V major opcode

<table>
<thead>
<tr>
<th>Function</th>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>funct6</td>
<td>31</td>
<td>Function</td>
</tr>
<tr>
<td>vm</td>
<td>26-25</td>
<td>Vector mask bit</td>
</tr>
<tr>
<td>vs2</td>
<td>20-19</td>
<td>Source vector register</td>
</tr>
<tr>
<td>vs1</td>
<td>15-14</td>
<td>Source register</td>
</tr>
<tr>
<td>vd</td>
<td>7-6</td>
<td>Destination register</td>
</tr>
<tr>
<td>0</td>
<td>0-0</td>
<td>Immediate data</td>
</tr>
</tbody>
</table>

Formats for Vector Configuration Instructions under OP-V major opcode
Vector instructions can have scalar or vector source operands and produce scalar or vector results, and most vector instructions can be performed either unconditionally or conditionally under a mask.

Vector loads and stores move bit patterns between vector register elements and memory. Vector arithmetic instructions operate on values held in vector register elements.

### 5.1. Scalar Operands

Scalar operands can be immediates, or taken from the x registers, the f registers, or element 0 of a vector register. Scalar results are written to an x or f register or to element 0 of a vector register. Any vector register can be used to hold a scalar regardless of the current LMUL setting.

In a change from v0.6, the floating-point registers no longer overlay the vector registers and scalars can now come from the integer or floating-point registers. Not overlaying the f registers reduces vector register pressure, avoids interactions with the standard calling convention, simplifies high-performance scalar floating-point design, and provides compatibility with the Zfnx ISA option. Overlaying f with v would provide the advantage of lowering the number of state bits in some implementations, but complicates high-performance designs and would prevent compatibility with the Zfnx ISA option.

### 5.2. Vector Operands

Each vector operand has an effective element width (EEW) and an effective LMUL (EMUL) that is used to determine the size and location of all the elements within a vector register group. By default, for most operands of most instructions, EEW=SEW and EMUL=LMUL.

Some vector instructions have source and destination vector operands with the same number of elements but different widths, so that EEW and EMUL differ from SEW and LMUL respectively but EEW/EMUL = SEW/LMUL. For example, most widening arithmetic instructions have a source group with EEW=SEW and EMUL=LMUL but destination group with EEW=2*SEW and EMUL=2*LMUL. Narrowing instructions have a source operand that has EEW=2*SEW and EMUL=2*LMUL but destination where EEW=SEW and EMUL=LMUL.

Vector operands or results may occupy one or more vector registers depending on EMUL, but are always specified using the lowest-numbered vector register in the group. Using other than the lowest-numbered vector register to specify a vector register group is a reserved encoding.

A destination vector register group can overlap a source vector register group only if one of the following holds:

- The destination EEW equals the source EEW.
- The destination EEW is smaller than the source EEW and the overlap is in the lowest-numbered part of the source register group (e.g., when LMUL=1, vnsrl.wi v0, v0, 3 is legal, but a destination of v1 is not).
- The destination EEW is greater than the source EEW, the source EMUL is at least 1, and the overlap is in the highest-numbered part of the destination register group (e.g., when LMUL=8, vzext.vf4 v0, v6 is legal, but a source of v0, v2, or v4 is not).

For the purpose of register group overlap constraints, mask elements have EEW=1.

The largest vector register group used by an instruction cannot be greater than 8 vector registers (i.e., EMUL≤8), and if a vector instruction would require greater than 8 vector registers in a group, the instruction encoding is reserved. For example, a widening operation that produces a widened vector register group result when LMUL=8 is reserved as this would imply a result EMUL=16.
Widened scalar values, e.g., results from widening reduction operations, are held in the first element of a vector register and have EMUL=1.

5.3. Vector Masking

Masking is supported on many vector instructions. Element operations that are masked off (inactive) never generate exceptions. The destination vector register elements corresponding to masked-off elements are handled with either a mask-undisturbed or mask-agnostic policy depending on the setting of the vma bit in vtype (Section Vector Tail Agnostic and Vector Mask Agnostic vta and vma).

In the base vector extension, the mask value used to control execution of a masked vector instruction is always supplied by vector register v0.

5.3.1. Mask Encoding

Where available, masking is encoded in a single-bit vm field in the instruction (inst[25]).

<table>
<thead>
<tr>
<th>vm</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>vector result, only where v0.mask[i] = 1</td>
</tr>
<tr>
<td>1</td>
<td>unmasked</td>
</tr>
</tbody>
</table>

Note: In earlier proposals, vm was a two-bit field vm[1:0] that provided both true and complement masking using v0 as well as encoding scalar operations.

Vector masking is represented in assembler code as another vector operand, with .t indicating if operation occurs when v0.mask[1] is 1. If no masking operand is specified, unmasked vector execution (vm=1) is assumed.

```
vop.v* v1, v2, v3, v0.t  # enabled where v0.mask[1]=1, m=0
vop.v* v1, v2, v3        # unmasked vector operation, m=1
```

Note: Even though the base only supports one vector mask register v0 and only the true form of predication, the assembly syntax writes it out in full to be compatible with future extensions that might add a mask register specifier and supporting both true and complement masking. The .t suffix on the masking operand also helps to visually encode the use of a mask.

The .mask suffix is not part of the assembly syntax. We only append it in contexts where a mask vector is subscripted, e.g., v0.mask[1].

5.4. Prestart, Active, Inactive, Body, and Tail Element Definitions
The destination element indices operated on during a vector instruction’s execution can be divided into three disjoint subsets.

- The **prestart** elements are those whose element index is less than the initial value in the \( v_{\text{start}} \) register. The prestart elements do not raise exceptions and do not update the destination vector register.

- The **body** elements are those whose element index is greater than or equal to the initial value in the \( v_{\text{start}} \) register, and less than the current vector length setting in \( v_{\text{l}} \). The body can be split into two disjoint subsets:
  - The **active** elements during a vector instruction’s execution are the elements within the body and where the current mask is enabled at that element position. The active elements can raise exceptions and update the destination vector register group.
  - The **inactive** elements are the elements within the body but where the current mask is disabled at that element position. The inactive elements do not raise exceptions and do not update any destination vector register group unless masked agnostic is specified (\( v_{\text{type}}.v_{\text{ma}}=1 \)), in which case inactive elements may be overwritten with 1s.

- The **tail** elements during a vector instruction’s execution are the elements past the current vector length setting specified in \( v_{\text{l}} \). The tail elements do not raise exceptions, and do not update any destination vector register group unless tail agnostic is specified (\( v_{\text{type}}.v_{\text{ta}}=1 \)), in which case tail elements may be overwritten with 1s. When \( \text{LMUL} < 1 \), the tail includes the elements past \( V_{\text{LMAX}} \) that are held in the same vector register.

```plaintext
for element index x
prestart = (0 <= x < v_{\text{start}})
body(x) = (v_{\text{start}} <= x < v_{\text{l}})
tail(x) = (v_{\text{l}} <= x < \max(V_{\text{LMAX}}, V_{\text{LEN}}/SEW))
mask(x) = \text{unmasked} || v_{\text{0.mask}}[x] == 1
active(x) = body(x) && mask(x)
inactive(x) = body(x) && !mask(x)
```

**Note**

Some instructions such as \( v_{\text{slidedown}} \) and \( v_{\text{rgather}} \) may read indices past \( v_{\text{l}} \) or even \( V_{\text{LMAX}} \) in source vector register groups. The general policy is to return the value 0 when the index is greater than \( V_{\text{LMAX}} \) in the source vector register group.
6. Configuration-Setting Instructions

One of the common approaches to handling a large number of elements is "stripmining" where each iteration of a loop handles some number of elements, and the iterations continue until all elements have been processed. The RISC-V vector specification provides direct, portable support for this approach. The application specifies the total number of elements to be processed (the application vector length or AVL) as a candidate value for $vl$, and the hardware responds via a general-purpose register with the (frequently smaller) number of elements that the hardware will handle per iteration (stored in $vl$), based on the microarchitectural implementation and the $vtype$ setting. A straightforward loop structure, shown in Example of stripmining and changes to SEW, depicts the ease with which the code keeps track of the remaining number of elements and the amount per iteration handled by hardware.

A set of instructions is provided to allow rapid configuration of the values in $vl$ and $vtype$ to match application needs.

6.1. vsetvli/vsetivli/vsetvl instructions

The vset{i}vl{i} instructions set the $vtype$ and $vl$ CSRs based on their arguments, and write the new value of $vl$ into $rd$.

```
vsetvli rd, rs1, vtypei   # rd = new vl, rs1 = AVL, vtypei = new vtype setting
vsetvli rd, uimm, vtypei # rd = new vl, uimm = AVL, vtypei = new vtype setting
vsetvl  rd, rs1, rs2     # rd = new vl, rs1 = AVL, rs2 = new vtype value
```

The new $vtype$ setting is encoded in the immediate fields of vsetvli and vsetivli, and in the rs2 register for vsetvl. The new vector length setting is based on AVL, which for vsetvli and vsetvl is encoded in the rs1 and rd fields as follows:

<table>
<thead>
<tr>
<th>rd</th>
<th>rs1</th>
<th>AVL value</th>
<th>Effect on vl</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>x0</td>
<td>Value in x[rs1]</td>
<td>Normal stripmining</td>
</tr>
<tr>
<td>lx0</td>
<td>x0</td>
<td>~0</td>
<td>Set vl to VLMAX</td>
</tr>
<tr>
<td>x0</td>
<td>x0</td>
<td>Value in vl register</td>
<td>Keep existing vl (of course, vtype may change)</td>
</tr>
</tbody>
</table>

When rs1 is not x0, the AVL is an unsigned integer held in the x register specified by rs1, and the new vl value is also written to the x register specified by rd.

When rs1=x0 but rd!=x0, the maximum unsigned integer value (~0) is used as the AVL, and the resulting VLMAX is written to vl and also to the x register specified by rd.

When rs1=x0 and rd=x0, the instruction operates as if the current vector length in vl is used as the AVL, and the resulting value is written to vl, but not to a destination register. This form can only be used when VLMAX and hence vl is not actually changed by the new SEW/LMUL ratio.

For the vsetivli instruction, the AVL is encoded as a 5-bit zero-extended immediate (0—31) in the rs1 field.

Note: The encoding of AVL for vsetivli is the same as for regular CSR immediate values.

Note: The vsetivli instruction provides more compact code when the dimensions of vectors are small, and known to fit inside the vector registers, so do not need stripmining overhead.

Use of the instruction with a new SEW/LMUL ratio that would result in a change of VLMAX is reserved. Implementations may set vll in this case.

Note: This last form of the instructions allows the $vtype$ register to be changed while maintaining the current $vl$, provided VLMAX is not reduced. This design was chosen to ensure $vl$ would always hold a legal value for current $vtype$ setting. The current $vl$ value can be read from the $vl$ CSR. The $vl$ value could be reduced by this instruction if the new SEW/LMUL ratio causes VLMAX to shrink, and so this case has been reserved as it is not clear this is a generally useful operation, and implementations can otherwise assume $vl$ is not changed by this instruction to optimize their microarchitecture.

Formats for Vector Configuration Instructions under OP-V major opcode
Table 8. vtype register layout

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XLEN-1</td>
<td>vill</td>
<td>Illegal value if set</td>
</tr>
<tr>
<td>XLEN-2:8</td>
<td></td>
<td>Reserved (write 0)</td>
</tr>
<tr>
<td>7</td>
<td>vma</td>
<td>Vector mask agnostic</td>
</tr>
<tr>
<td>6</td>
<td>vta</td>
<td>Vector tail agnostic</td>
</tr>
<tr>
<td>5:3</td>
<td>vsew[2:0]</td>
<td>Selected element width (SEW) setting</td>
</tr>
<tr>
<td>2:0</td>
<td>vlmul[2:0]</td>
<td>Vector register group multiplier (LMUL) setting</td>
</tr>
</tbody>
</table>

Suggested assembler names used for vsetvli immediate

```
    e8    # SEW=8b
    e16   # SEW=16b
    e32   # SEW=32b
    e64   # SEW=64b
    e128  # SEW=128b
    e256  # SEW=256b
    e512  # SEW=512b
    e1024 # SEW=1024b
    mf8   # LMUL=1/8
    mf4   # LMUL=1/4
    mf2   # LMUL=1/2
    m1    # LMUL=1, assumed if m setting absent
    m2    # LMUL=2
    m4    # LMUL=4
    m8    # LMUL=8
```

Examples:
```
vsetvli t0, a0, e8          # SEW= 8, LMUL=1
vsetvli t0, a0, e8,m2       # SEW= 8, LMUL=2
vsetvli t0, a0, e32,mf2     # SEW=32, LMUL=1/2
```

The vsetvl variant operates similarly to vsetvli except that it takes a vtype value from rs2 and can be used for context restore.

If the vtype setting is not supported by the implementation, then the vill bit is set in vtype, the remaining bits in vtype are set to zero, and the vl register is also set to zero.

Note: Earlier drafts required a trap when setting vtype to an illegal value. However, this would have added the first data-dependent trap on a CSR write to the ISA. Implementations may choose to trap when illegal values are written to vtype instead of setting vill, to allow emulation to support new configurations for forward-compatibility. The current scheme supports light-weight runtime interrogation of the supported vector unit configurations by checking if vill is clear for a given setting.

6.2. Constraints on Setting vl

The vset{i}vl{i} instructions first set VLMAX according to the vtype argument, then set vl obeying the following constraints:

1. vl = AVL if AVL ≤ VLMAX
2. \(\text{ceil}(\text{AVL} / 2) \leq v_l \leq \text{VLMAX} \text{if AVL} < (2 \times \text{VLMAX})\)

3. \(v_l = \text{VLMAX} \text{if AVL} \geq (2 \times \text{VLMAX})\)

4. Deterministic on any given implementation for same input AVL and VLMAX values

5. These specific properties follow from the prior rules:
   a. \(v_l = 0 \text{if AVL} = 0\)
   b. \(v_l > 0 \text{if AVL} > 0\)
   c. \(v_l \leq \text{VLMAX}\)
   d. \(v_l \leq \text{AVL}\)
   e. A value read from \(v_l\) when used as the AVL argument to \(v\text{set\{i\}v\{i\}}\) results in the same value in \(v_l\), provided the resultant VLMAX equals the value of VLMAX at the time that \(v_l\) was read

The \(v_l\) setting rules are designed to be sufficiently strict to preserve \(v_l\) behavior across register spills and context swaps for \(\text{AVL} \leq \text{VLMAX}\), yet flexible enough to enable implementations to improve vector lane utilization for \(\text{AVL} > \text{VLMAX}\). For example, this permits an implementation to set \(v_l = \text{ceil}(\text{AVL} / 2)\) for \(\text{VLMAX} < \text{AVL} < 2^\times\text{VLMAX}\) in order to evenly distribute work over the last two iterations of a stripmine loop. Requirement 2 ensures that the first stripmine iteration of reduction loops uses the largest vector length of all iterations, even in the case of \(\text{AVL} < 2^\times\text{VLMAX}\). This allows software to avoid needing to explicitly calculate a running maximum of vector lengths observed during a stripmined loop.

### 6.3. Example of stripmining and changes to SEW

The SEW and LMUL settings can be changed dynamically to provide high throughput on mixed-width operations in a single loop.

```
# Example: Load 16-bit values, widen multiply to 32b, shift 32b result
# right by 3, store 32b values.
# On entry:
#  a0 holds the total number of elements to process
#  a1 holds the address of the source array
#  a2 holds the address of the destination array
loop:
  vsetvl1 a3, a0, e16,m4,ta,ma  # vtype = 16-bit integer vectors;
  vle16.v v4, (a1)        # Get 16b vector
  slli t1, a3, 1          # Multiply # elements this iteration by 2 bytes/source element
  add a1, a1, t1          # Bump pointer
  vwmul.vx v8, v4, x10    # Widening multiply into 32b in <v8--v15>
  vsetvl1 x8, x0, e32,m8,ta,ma  # Operate on 32b values
  vsr1.vi v8, v8, 3
  vse32.v v8, (a2)        # Store vector of 32b elements
  slli t1, a3, 2          # Multiply # elements this iteration by 4 bytes/destination element
  add a2, a2, t1          # Bump pointer
  sub a0, a0, a3          # Decrement count by v_l
  bnez a0, loop           # Any more?
```
7. Vector Loads and Stores

Vector loads and stores move values between vector registers and memory. Vector loads and stores are masked and do not raise exceptions on inactive elements. Masked vector loads do not update inactive elements in the destination vector register group, unless masked agnostic is specified (vtype, vma=1). Masked vector stores only update active memory elements. All vector loads and stores may generate and accept a non-zero vstart value.

7.1. Vector Load/Store Instruction Encoding

Vector loads and stores are encoded within the scalar floating-point load and store major opcodes (LOAD-FP/STORE-FP). The vector load and store encodings repurpose a portion of the standard scalar floating-point load/store 12-bit immediate field to provide further vector instruction encoding, with bit 25 holding the standard vector mask bit (see Mask Encoding).

Format for Vector Load Instructions under LOAD-FP major opcode

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>rs1[4:0]</td>
<td>specifies x register holding base address</td>
</tr>
<tr>
<td>rs2[4:0]</td>
<td>specifies x register holding stride</td>
</tr>
<tr>
<td>vs2[4:0]</td>
<td>specifies v register holding address offsets</td>
</tr>
<tr>
<td>vs3[4:0]</td>
<td>specifies v register holding store data</td>
</tr>
<tr>
<td>vd[4:0]</td>
<td>specifies v register destination of load</td>
</tr>
<tr>
<td>vm</td>
<td>specifies whether vector masking is enabled (0 = mask enabled, 1 = mask disabled)</td>
</tr>
<tr>
<td>width[2:0]</td>
<td>specifies size of memory elements, and distinguishes from FP scalar</td>
</tr>
<tr>
<td>mew</td>
<td>extended memory element width. See Vector Load/Store Width Encoding</td>
</tr>
<tr>
<td>mop[1:0]</td>
<td>specifies memory addressing mode</td>
</tr>
<tr>
<td>nf[2:0]</td>
<td>specifies the number of fields in each segment, for segment load/stores</td>
</tr>
<tr>
<td>lumop[4:0]/sumop[4:0]</td>
<td>are additional fields encoding variants of unit-stride instructions</td>
</tr>
</tbody>
</table>

Vector memory unit-stride and constant-stride operations directly encode EEW of the data to be transferred statically in the instruction to reduce the number of vtype changes when accessing memory in a mixed-width routine. Indexed operations use the explicit EEW encoding in the instruction to set the size of the indices used, and use SEW/LMUL to specify the data width.

7.2. Vector Load/Store Addressing Modes

The base vector extension supports unit-stride, strided, and indexed (scatter/gather) addressing modes. Vector load/store base registers and strides are taken from the GPR x registers.
The base effective address for all vector accesses is given by the contents of the x register named in rs1.

Vector unit-stride operations access elements stored contiguously in memory starting from the base effective address.

Vector constant-strided operations access the first memory element at the base effective address, and then access subsequent elements at address increments given by the byte offset contained in the x register specified by rs2.

Vector indexed operations add the contents of each element of the vector offset operand specified by vs2 to the base effective address to give the effective address of each element. The data vector register group has EEW=SEW, EMUL=LMUL, while the offset vector register group has EEW encoding in the instruction and EMUL=(EEW/SEW)*LMUL.

The vector offset operand is treated as a vector of byte-address offsets.

The indexed operations can also be used to access fields within a vector of objects, where the vs2 vector holds pointers to the base of the objects and the scalar x register holds the offset of the member field in each object. Supporting this case is why the indexed operations were not defined to scale the element indices by the data EEW.

If the vector offset elements are narrower than XLEN, they are zero-extended to XLEN before adding to the base effective address. If the vector offset elements are wider than XLEN, the least-significant XLEN bits are used in the address calculation.

A profile may place a upper limit on the maximum required index EEW (e.g., only up to XLEN) smaller than ELEN, in which case an illegal instruction exception can be raised if the EEW is not supported.

The vector addressing modes are encoded using the 2-bit mop [1:0] field.

Table 9. encoding for loads

<table>
<thead>
<tr>
<th>mop [1:0]</th>
<th>Description</th>
<th>Opcodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>unit-stride</td>
<td>VLE&lt;EEW&gt;</td>
</tr>
<tr>
<td>0 1</td>
<td>indexed-unordered</td>
<td>VLUXEI&lt;EEW&gt;</td>
</tr>
<tr>
<td>1 0</td>
<td>strided</td>
<td>VLSE&lt;EEW&gt;</td>
</tr>
<tr>
<td>1 1</td>
<td>indexed-ordered</td>
<td>VLOXEI&lt;EEW&gt;</td>
</tr>
</tbody>
</table>

Table 10. encoding for stores

<table>
<thead>
<tr>
<th>mop [1:0]</th>
<th>Description</th>
<th>Opcodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>unit-stride</td>
<td>VSE&lt;EEW&gt;</td>
</tr>
<tr>
<td>0 1</td>
<td>indexed-unordered</td>
<td>VSUXEI&lt;EEW&gt;</td>
</tr>
<tr>
<td>1 0</td>
<td>strided</td>
<td>VSSE&lt;EEW&gt;</td>
</tr>
<tr>
<td>1 1</td>
<td>indexed-ordered</td>
<td>VSOXEI&lt;EEW&gt;</td>
</tr>
</tbody>
</table>

Vector unit-stride and constant-stride memory accesses do not guarantee ordering between individual element accesses. The vector indexed load and store memory operations have two forms, ordered and unordered. The indexed-ordered variants preserve element ordering on memory accesses.

For unordered instructions (mop!=11) there is no guarantee on element access order. If the accesses are to a strongly ordered IO region, the element accesses can be initiated in any order.

To provide ordered vector accesses to a strongly ordered IO region, the ordered indexed instructions should be used.

For implementations with precise vector traps, exceptions on indexed-unordered stores must also be precise.

Additional unit-stride vector addressing modes are encoded using the 5-bit lumop and sumop fields in the unit-stride load and store instruction encodings respectively.
### Table 11. lumop

<table>
<thead>
<tr>
<th>lumop[4:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 0 0</td>
<td>unit-stride</td>
</tr>
<tr>
<td>0 0 x 0 1 0</td>
<td>reserved</td>
</tr>
<tr>
<td>0 0 x 1 0 0</td>
<td>reserved</td>
</tr>
<tr>
<td>0 1 0 1 1 1</td>
<td>unit-stride, mask load, EEW=1</td>
</tr>
<tr>
<td>0 1 0 0 0 0</td>
<td>unit-stride, whole registers</td>
</tr>
<tr>
<td>0 1 x x x 0</td>
<td>reserved, x !=0</td>
</tr>
<tr>
<td>1 0 0 0 0 0</td>
<td>unit-stride fault-only-first</td>
</tr>
<tr>
<td>1 x x x x x</td>
<td>reserved, x !=0</td>
</tr>
</tbody>
</table>

### Table 12. sumop

<table>
<thead>
<tr>
<th>sumop[4:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 0 0</td>
<td>unit-stride</td>
</tr>
<tr>
<td>0 0 x 0 1 0</td>
<td>reserved</td>
</tr>
<tr>
<td>0 0 x 1 0 0</td>
<td>reserved</td>
</tr>
<tr>
<td>0 1 0 1 1 1</td>
<td>unit-stride, mask store, EEW=1</td>
</tr>
<tr>
<td>0 0 x x x 0</td>
<td>reserved, x !=0</td>
</tr>
<tr>
<td>0 1 0 0 0 0</td>
<td>unit-stride, whole registers</td>
</tr>
<tr>
<td>0 1 x x x 0</td>
<td>reserved, x !=0</td>
</tr>
<tr>
<td>1 x x x x x</td>
<td>reserved</td>
</tr>
</tbody>
</table>

The nf[2:0] field encodes the number of fields in each segment. For regular vector loads and stores, nf=0, indicating that a single value is moved between a vector register group and memory at each element position. Larger values in the nf field are used to access multiple contiguous fields within a segment as described below in Section Vector Load/Store Segment Instructions.

**Note:** nf field for segment load/stores has replaced the use of the same bits for an address offset field. The offset can be replaced with a single scalar integer calculation, while segment load/stores add more powerful primitives to move items to and from memory.

The nf[2:0] field also encodes the number of whole vector registers to transfer for the whole vector register load/store instructions.

### 7.3. Vector Load/Store Width Encoding

Vector loads and stores have an EEW encoded directly in the instruction. The corresponding EMUL is calculated as EMUL = (EEW/SEW)*LMUL. If the EMUL would be out of range (EMUL>8 or EMUL<1/8), the instruction encoding is reserved. The vector register groups must have legal register specifiers for the selected EMUL; the instruction encoding is otherwise considered reserved.

Vector unit-stride and constant-stride use the EEW/EMUL encoded in the instruction for the data values, while vector indexed loads and stores use the EEW/EMUL encoded in the instruction for the index values and the SEW/LMUL encoded in vtype for the data values.

Vector loads and stores are encoded using width values that are not claimed by the standard scalar floating-point loads and stores.

The mew bit (inst[28]) is expected to be used to encode expanded memory sizes of 128 bits and above, but these encodings are reserved at this point.

Vector loads and stores for EEWs of all supported SEW settings must be provided in an implementation. Vector load/store encodings for unsupported EEW widths are reserved.
Table 13. Width encoding for vector loads and stores.

<table>
<thead>
<tr>
<th>Mem bits</th>
<th>Data Reg bits</th>
<th>Index bits</th>
<th>Opcodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard scalar FP</td>
<td>16</td>
<td>FLEN</td>
<td>FLH/FSH</td>
</tr>
<tr>
<td>Standard scalar FP</td>
<td>32</td>
<td>FLEN</td>
<td>FLW/FSW</td>
</tr>
<tr>
<td>Standard scalar FP</td>
<td>64</td>
<td>FLEN</td>
<td>FLD/FSD</td>
</tr>
<tr>
<td>Standard scalar FP</td>
<td>128</td>
<td>FLEN</td>
<td>FLQ/FSQ</td>
</tr>
<tr>
<td>Vector 8b element</td>
<td>8</td>
<td>8</td>
<td>VLxE8/VSxE8</td>
</tr>
<tr>
<td>Vector 16b element</td>
<td>16</td>
<td>16</td>
<td>VLxE16/VSxE16</td>
</tr>
<tr>
<td>Vector 32b element</td>
<td>32</td>
<td>32</td>
<td>VLxE32/VSxE32</td>
</tr>
<tr>
<td>Vector 64b element</td>
<td>64</td>
<td>64</td>
<td>VLxE64/VSxE64</td>
</tr>
<tr>
<td>Vector 128b element</td>
<td>128</td>
<td>128</td>
<td>VLxE128/VSxE128 Reserved</td>
</tr>
<tr>
<td>Vector 256b element</td>
<td>256</td>
<td>256</td>
<td>VLxE256/VSxE256 Reserved</td>
</tr>
<tr>
<td>Vector 512b element</td>
<td>512</td>
<td>512</td>
<td>VLxE512/VSxE512 Reserved</td>
</tr>
<tr>
<td>Vector 1024b element</td>
<td>1024</td>
<td>1024</td>
<td>VLxE1024/VSxE1024 Reserved</td>
</tr>
<tr>
<td>Vector 8b index</td>
<td>SEW</td>
<td>SEW</td>
<td>8</td>
</tr>
<tr>
<td>Vector 16b index</td>
<td>SEW</td>
<td>SEW</td>
<td>16</td>
</tr>
<tr>
<td>Vector 32b index</td>
<td>SEW</td>
<td>SEW</td>
<td>32</td>
</tr>
<tr>
<td>Vector 64b index</td>
<td>SEW</td>
<td>SEW</td>
<td>64</td>
</tr>
</tbody>
</table>

Mem bits is the size of each element accessed in memory.

Data reg bits is the size of each data element accessed in register.

Index bits is the size of each index accessed in register.

Note: In base V extension, only data elements widths up to max(XLEN,FLEN) must be supported.

7.4. Vector Unit-Stride Instructions
# Vector unit-stride loads and stores

# vd destination, rs1 base address, vm is mask encoding (v0.t or <missing>)
vl8.v vd, (rs1), vm # 8-bit unit-stride load
vl16.v vd, (rs1), vm # 16-bit unit-stride load
vl32.v vd, (rs1), vm # 32-bit unit-stride load
vl64.v vd, (rs1), vm # 64-bit unit-stride load
# vl128.v vd, (rs1), vm # 128-bit unit-stride load. Reserved
# vl256.v vd, (rs1), vm # 256-bit unit-stride load. Reserved
# vl512.v vd, (rs1), vm # 512-bit unit-stride load. Reserved
# vl1024.v vd, (rs1), vm # 1024-bit unit-stride load. Reserved

# vs3 store data, rs1 base address, vm is mask encoding (v0.t or <missing>)
vse8.v vs3, (rs1), vm # 8-bit unit-stride store
vse16.v vs3, (rs1), vm # 16-bit unit-stride store
vse32.v vs3, (rs1), vm # 32-bit unit-stride store
vse64.v vs3, (rs1), vm # 64-bit unit-stride store
# vse128.v vs3, (rs1), vm # 128-bit unit-stride store. Reserved
# vse256.v vs3, (rs1), vm # 256-bit unit-stride store. Reserved
# vse512.v vs3, (rs1), vm # 512-bit unit-stride store. Reserved
# vse1024.v vs3, (rs1), vm # 1024-bit unit-stride store. Reserved

An additional unit-stride load and store is provided to support transferring mask values (EEW=1) to/from memory. These operate the same as unmasked byte loads or stores, except that the effective vector length is evl=ceil(vl/8), and the destination register is always written with a tail-agnostic policy.

# Vector unit-stride mask load
vle1.v vd, (rs1) # Load byte vector of length ceil(vl/8)

# Vector unit-stride mask store
vse1.v vs3, (rs1) # Store byte vector of length ceil(vl/8)

Note
The primary motivation to provide mask load and store is to support machines that internally rearrange data based on EEW to reduce cross-datapath wiring. However, this also provides a convenient mechanism to access packed bit vectors in memory as mask registers, and reduces the cost of mask spill/fill by reducing need to change v1.

7.5. Vector Strided Instructions

# Vector strided loads and stores

# vd destination, rs1 base address, rs2 byte stride
vlse8.v vd, (rs1), rs2, vm # 8-bit strided load
vlse16.v vd, (rs1), rs2, vm # 16-bit strided load
vlse32.v vd, (rs1), rs2, vm # 32-bit strided load
vlse64.v vd, (rs1), rs2, vm # 64-bit strided load
# vlse128.v vd, (rs1), rs2, vm # 128-bit strided load. Reserved
# vlse256.v vd, (rs1), rs2, vm # 256-bit strided load. Reserved
# vlse512.v vd, (rs1), rs2, vm # 512-bit strided load. Reserved
# vlse1024.v vd, (rs1), rs2, vm # 1024-bit strided load. Reserved

# vs3 store data, rs1 base address, rs2 byte stride
vsse8.v vs3, (rs1), rs2, vm # 8-bit strided store
vsse16.v vs3, (rs1), rs2, vm # 16-bit strided store
vsse32.v vs3, (rs1), rs2, vm # 32-bit strided store
vsse64.v vs3, (rs1), rs2, vm # 64-bit strided store
# vsse128.v vs3, (rs1), rs2, vm # 128-bit strided store. Reserved
# vsse256.v vs3, (rs1), rs2, vm # 256-bit strided store. Reserved
# vsse512.v vs3, (rs1), rs2, vm # 512-bit strided store. Reserved
# vsse1024.v vs3, (rs1), rs2, vm # 1024-bit strided store. Reserved
Negative and zero strides are supported.

Element accesses within a strided instruction are unordered with respect to each other.

When rs2=x0, then an implementation is allowed, but not required, to perform fewer memory operations than the number of active elements, and may perform different numbers of memory operations across different dynamic executions of the same static instruction.

Note: Compilers must be aware to not use the x0 form for rs2 when the immediate stride is 0 if the intent to is to require all memory accesses are performed.

When rs2!=x0 and the value of x[rs2]=0, the implementation must perform one memory access for each active element (but these accesses will not be ordered).

Note: When repeating ordered vector accesses to the same memory address are required, then an ordered indexed operation can be used.

### 7.6. Vector Indexed Instructions

```
# Vector unordered indexed load instructions
# vd destination, rs1 base address, vs2 indices
vluxe8.v vd, (rs1), vs2, vm # unordered 8-bit indexed load of SEW data
vluxe16.v vd, (rs1), vs2, vm # unordered 16-bit indexed load of SEW data
vluxe32.v vd, (rs1), vs2, vm # unordered 32-bit indexed load of SEW data
vluxe64.v vd, (rs1), vs2, vm # unordered 64-bit indexed load of SEW data

# Vector ordered indexed load instructions
# vd destination, rs1 base address, vs2 indices
vloxei8.v vd, (rs1), vs2, vm # ordered 8-bit indexed load of SEW data
vloxei16.v vd, (rs1), vs2, vm # ordered 16-bit indexed load of SEW data
vloxei32.v vd, (rs1), vs2, vm # ordered 32-bit indexed load of SEW data
vloxei64.v vd, (rs1), vs2, vm # ordered 64-bit indexed load of SEW data

# Vector unordered-indexed store instructions
# vs3 store data, rs1 base address, vs2 indices
vsuxei8.v vs3, (rs1), vs2, vm # unordered 8-bit indexed store of SEW data
vsuxei16.v vs3, (rs1), vs2, vm # unordered 16-bit indexed store of SEW data
vsuxei32.v vs3, (rs1), vs2, vm # unordered 32-bit indexed store of SEW data
vsuxei64.v vs3, (rs1), vs2, vm # unordered 64-bit indexed store of SEW data

# Vector ordered indexed store instructions
# vs3 store data, rs1 base address, vs2 indices
vsoxei8.v vs3, (rs1), vs2, vm # ordered 8-bit indexed store of SEW data
vsoxei16.v vs3, (rs1), vs2, vm # ordered 16-bit indexed store of SEW data
vsoxei32.v vs3, (rs1), vs2, vm # ordered 32-bit indexed store of SEW data
vsoxei64.v vs3, (rs1), vs2, vm # ordered 64-bit indexed store of SEW data
```

Note: The assembler syntax for indexed loads and stores uses eix instead of ex to indicate the statically encoded EEW is of the index not the data.

The indexed operations mnemonics have a "U" or "O" to distinguish between unordered and ordered, while the other vector addressing modes have no character. While this is perhaps a little less consistent, this approach minimizes disruption to existing software, as VSXEI previously meant "ordered" - and the opcode can be retained as an alias during transition to help reduce software churn.

### 7.7. Unit-stride Fault-Only-First Loads

The unit-stride fault-only-first load instructions are used to vectorize loops with data-dependent exit conditions ("while" loops). These instructions execute as a regular load except that they will only take a trap caused by a synchronous exception on element 0. If element 0 raises an exception, v1 is not modified, and the trap is taken. If an element > 0 raises an
exception, the corresponding trap is not taken, and the vector length $vl$ is reduced to the index of the element that would have raised an exception.

Load instructions may overwrite active destination vector register group elements past the element index at which the trap is reported. Similarly, fault-only-first load instructions may update destination elements past the element that causes trimming of the vector length (but not past the original vector length). The values of these spurious updates do not have to correspond to the values in memory at the addressed memory locations. Non-idempotent memory locations can only be accessed when it is known the corresponding element load operation will not be restarted due to a trap or vector length trimming.

# Vector unit-stride fault-only-first loads

```assembly
# vd destination, rs1 base address, vm is mask encoding (v0.t or <missing>)
vle8ff.v vd, (rs1), vm  # 8-bit unit-stride fault-only-first load
vle16ff.v vd, (rs1), vm  # 16-bit unit-stride fault-only-first load
vle32ff.v vd, (rs1), vm  # 32-bit unit-stride fault-only-first load
vle64ff.v vd, (rs1), vm  # 64-bit unit-stride fault-only-first load
# vle128ff.v vd, (rs1), vm  # 128-bit unit-stride fault-only-first load. Reserved
# vle256ff.v vd, (rs1), vm  # 256-bit unit-stride fault-only-first load. Reserved
# vle512ff.v vd, (rs1), vm  # 512-bit unit-stride fault-only-first load. Reserved
# vle1024ff.v vd, (rs1), vm  # 1024-bit unit-stride fault-only-first load. Reserved
```

`strlen` example using unit-stride fault-only-first instruction

```assembly
# size_t strlen(const char *str)
# a0 holds *str

strlen:
   mv a3, a0              # Save start

loop:
   vsetvli a1, x0, e8, m8, ta, ma  # Vector of bytes of maximum length
   vle8ff.v v8, (a3)      # Load bytes
   csrr a1, vl           # Get bytes read
   vmseq.vi v0, v8, 0    # Set v0[i] where v8[i] = 0
   vfirst.m a2, v0       # Find first set bit
   add a3, a3, a1        # Bump pointer
   bltz a2, loop         # Not found?
   add a0, a0, a1        # Sum start + bump
   add a3, a3, a2        # Add index
   sub a0, a3, a0        # Subtract start address+bump

ret
```

Note: When the fault-only-first instruction would trigger a debug data-watchpoint trap on an element after the first, implementations should not reduce $vl$ but instead should trigger the debug trap as otherwise the event might be lost.

7.8. Vector Load/Store Segment Instructions
This instruction subset is given the ISA string name Zv1seg.

**Note** This set of instructions is included in the base "V" extension used for the Unix profile.

The vector load/store segment instructions move multiple contiguous fields in memory to and from consecutively numbered vector registers.

**Note** These operations support operations on "array-of-structures" datatypes by unpacking each field in a structure into separate vector registers.

The three-bit nf field in the vector instruction encoding is an unsigned integer that contains one less than the number of fields per segment, NFIELDS.

<table>
<thead>
<tr>
<th>nf[2:0]</th>
<th>NFIELDS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>1</td>
</tr>
<tr>
<td>0 0 1</td>
<td>2</td>
</tr>
<tr>
<td>0 1 0</td>
<td>3</td>
</tr>
<tr>
<td>0 1 1</td>
<td>4</td>
</tr>
<tr>
<td>1 0 0</td>
<td>5</td>
</tr>
<tr>
<td>1 0 1</td>
<td>6</td>
</tr>
<tr>
<td>1 1 0</td>
<td>7</td>
</tr>
<tr>
<td>1 1 1</td>
<td>8</td>
</tr>
</tbody>
</table>

The EMUL setting must be such that EMUL * NFIELDS ≤ 8, otherwise the instruction encoding is reserved.

**Note** The product EMUL * NFIELDS represents the number of underlying vector registers that will be touched by a segmented load or store instruction. This constraint makes this total no larger than 1/4 of the architectural register file, and the same as for regular operations with EMUL=8.

Each field will be held in successively numbered vector register groups. When EMUL>1, each field will occupy a vector register group held in multiple successively numbered vector registers, and the vector register group for each field must follow the usual vector register alignment constraints (e.g., when EMUL=2 and NFIELDS=4, each field's vector register group must start at an even vector register, but does not have to start at a multiple of 8 vector register number).

If the vector register numbers accessed by the segment load or store would increment past 31, then the instruction encoding is reserved.

**Note** This constraint is to help allow for forward-compatibility with a possible future longer instruction encoding that has more addressable vector registers.

The vl register gives the number of structures to move, which is equal to the number of elements transferred to each vector register group. Masking is also applied at the level of whole structures.

For segment loads and stores, the individual memory accesses used to access fields within each segment are unordered with respect to each other even for ordered indexed segment loads and stores.

If a trap is taken, vstart is in units of structures. If a trap occurs partway through accessing a structure, it is implementation-defined whether a subset of the structure access is performed.

**7.8.1. Vector Unit-Stride Segment Loads and Stores**

The vector unit-stride load and store segment instructions move packed contiguous segments ("array-of-structures") into multiple destination vector register groups.

**Note** For structures with heterogeneous-sized fields, software can later unpack structure fields from a segment using additional instructions after the segment load brings data into the vector registers.

The assembler prefixes v1seg/vsseg are used for unit-stride segment loads and stores respectively.
### Format

vlseg<nf>e<eew>.v vd, (rs1), vm # Unit-stride segment load template
vsseg<nf>e<eew>.v vs3, (rs1), vm # Unit-stride segment store template

### Examples

vlseg8e8.v vd, (rs1), vm # Load eight vector registers with eight byte fields.

vsseg3e32.v vs3, (rs1), vm # Store packed vector of 3*4-byte segments from vs3, vs3+1, vs3+2 to mem

For loads, the \( vd \) register will hold the first field loaded from the segment. For stores, the \( vs3 \) register is read to provide the first field to be stored in each segment.

### Example 1

- Memory structure holds packed RGB pixels (24-bit data structure, 8bpp)
- \( v8 \) holds the red pixels
- \( v9 \) holds the green pixels
- \( v10 \) holds the blue pixels

### Example 2

- Memory structure holds complex values, 32b for real and 32b for imaginary
- \( v8 \) holds real
- \( v9 \) holds imaginary

There are also fault-only-first versions of the unit-stride instructions.

### Template for vector fault-only-first unit-stride segment loads.

vlseg<nf>e<eew>ff.v vd, (rs1), vm # Unit-stride fault-only-first segment loads

These instructions may overwrite destination vector register group elements past the point at which a trap is reported or past the point at which vector length is trimmed.

### 7.8.2. Vector Strided Segment Loads and Stores

Vector strided segment loads and stores move contiguous segments where each segment is separated by the byte-stride offset given in the \( rs2 \) GPR argument.

Note Negative and zero strides are supported.

### Format

vlsseg<nf>e<eew>.v vd, (rs1), rs2, vm # Strided segment loads
vssseg<nf>e<eew>.v vs3, (rs1), rs2, vm # Strided segment stores

### Examples

vsetvli a1, t0, e8, ta, ma
vlsseg3e8.v v8, (a0), vm # v8 holds the red pixels
vssseg3e32.v vs3, (rs1), vm # Load bytes at addresses x5+i*x6 into v4[i],
# and bytes at addresses x5+i*x6+1 into v5[i],
# and bytes at addresses x5+i*x6+2 into v6[i].

### Examples

vsetvli a1, t0, e32, ta, ma
vssseg2e32.v v2, (x5), x6 # Store words from v2[i] to address x5+i*x6
# and words from v3[i] to address x5+i*x6+4

Accesses to the fields within each segment can occur in any order, including the case where the byte stride is such that segments overlap in memory.
7.8.3. Vector Indexed Segment Loads and Stores

Vector indexed segment loads and stores move contiguous segments where each segment is located at an address given by adding the scalar base address in the rs1 field to byte offsets in vector register vs2. Both ordered and unordered forms are provided, where the ordered forms access segments in element order. However, even for the ordered form, accesses to the fields within an individual segment are not ordered with respect to each other.

The data vector register group has EEW=SEW, EMUL=LMUL, while the index vector register group has EEW encoded in the instruction with EMUL=(EEW/SEW)*LMUL.

### Format

vluxseg<nf>ei<eew>.v vd, (rs1), vs2, vm # Unordered indexed segment loads
vloxseg<nf>ei<eew>.v vd, (rs1), vs2, vm # Ordered indexed segment loads
vsuxseg<nf>ei<eew>.v vs3, (rs1), vs2, vm # Unordered indexed segment stores
vsoxseg<nf>ei<eew>.v vs3, (rs1), vs2, vm # Ordered indexed segment stores

### Examples

vsetvli a1, t0, e8, ta, ma
vluxseg3ei32.v v4, (x5), v3 # Load bytes at addresses x5+v3[i] into v4[i],
# and bytes at addresses x5+v3[i]+1 into v5[i],
# and bytes at addresses x5+v3[i]+2 into v6[i].

vsetvli a1, t0, e32, ta, ma
vsuxseg2ei32.v v2, (x5), v5 # Store words from v2[i] to address x5+v5[i]
# and words from v3[i] to address x5+v5[i]+4

For vector indexed segment loads, the destination vector register groups cannot overlap the source vector register group (specified by vs2), else the instruction encoding is reserved.

Note: This constraint supports restart of indexed segment loads that raise exceptions partway through loading a structure.

7.9. Vector Load/Store Whole Register Instructions

Format for Vector Load Whole Register Instructions under LOAD-FP major opcode

| 31 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| nf | mew | 0  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  |
|    | mop | vm | lunop | base address | destination of load |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| nf | 0  | 0  | 0  | 1  | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 0  | 0  | 0  |
|    | mop | vm | lunop | base address | store data |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

These instructions load and store whole vector register groups.

Note: These instructions are intended to be used to save and restore vector registers when the type or length of the current contents of the vector register is not known, or where modifying vl and vtype would be costly. Examples include compiler register spills, vector function calls where values are passed in vector registers, interrupt handlers, and OS context switches. Software can determine the number of bytes transferred by reading the vlenb register.

The load instructions have an EEW encoded in the mew and width fields following the pattern of regular unit-stride loads. Because in-register byte layouts are identical to in-memory byte layouts, these instructions all operate the same as moving vectors of bytes with EEW=8, regardless of actual EEW encoding. Pseudo-instructions are provide for whole register load instructions that correspond to EEW=8.

Note: For the purposes of opaque save and restore of register state, the instructions have been defined as only moving byte vectors (SEW=8) between registers and memory.

The encoded EEW can be used as a HINT to indicate the destination register group will next be accessed with this EEW, which aids implementations that rearrange data internally.

The vector whole register store instructions are encoded similar to unmasked unit-stride store of elements with EEW=8.
The nf field encodes how many vector registers to load and store. The encoded number of registers must be a power of 2 and the vector register numbers must be aligned as with a vector register group, otherwise the instruction encoding is reserved. The nf field encodes the number of vector registers to transfer, numbered successively after the base. Only nf values of 1, 2, 4, 8 are supported, with other values reserved. When multiple registers are transferred, the lowest-numbered vector register is held in the lowest-numbered memory addresses and successive vector register numbers are placed contiguously in memory.

The instructions operate with an effective vector length, evl= nf*VLEN/EEW, regardless of current settings in vtype and vl. The usual property that no elements are written if vstart ≥ vl does not apply to these instructions. Instead, no elements are written if vstart ≥ evl.

The instructions operate similarly to unmasked unit-stride load and store instructions of elements, with the base address passed in the scalar x register specified by rs1.

Implementations are allowed to raise a misaligned address exception on whole register loads and stores if the base address is not naturally aligned to the larger of the size of the encoded EEW in bytes (EEW/8) or the implementation’s smallest supported SEW size in bytes (SEW_MIN/8).

Note: Allowing misaligned exceptions to be raised based on non-alignment to encoded EEW simplifies the implementation of these instructions. Some implementations might not support smaller SEW widths, so are allowed to report misaligned exceptions for the smallest supported SEW even if larger than encoded EEW. An extreme implementation might have SEW_MIN > XLEN for example. Software environments can mandate the minimum alignment requirements to support an ABI. The base V extension mandates support for SEW=8.
Format of whole register load and store instructions.

vl1r.v v3, (a0)  # Pseudo instruction equal to vl1re8.v
vl1re8.v v3, (a0)  # Load v3 with VLEN/8 bytes held at address in a0
vl1re16.v v3, (a0)  # Load v3 with VLEN/16 halfwords held at address in a0
vl1re32.v v3, (a0)  # Load v3 with VLEN/32 words held at address in a0
vl1re64.v v3, (a0)  # Load v3 with VLEN/64 doublewords held at address in a0
vl1re128.v v3, (a0)
vl1re256.v v3, (a0)
vl1re512.v v3, (a0)
vl1re1024.v v3, (a0)

vl2r.v v2, (a0)  # Pseudo instruction equal to vl2re8.v v2, (a0)
vl2re8.v v2, (a0)  # Load v2-v3 with 2*VLEN/8 bytes from address in a0
vl2re16.v v2, (a0)  # Load v2-v3 with 2*VLEN/16 halfwords held at address in a0
vl2re32.v v2, (a0)  # Load v2-v3 with 2*VLEN/32 words held at address in a0
vl2re64.v v2, (a0)  # Load v2-v3 with 2*VLEN/64 doublewords held at address in a0
vl2re128.v v2, (a0)
vl2re256.v v2, (a0)
vl2re512.v v2, (a0)
vl2re1024.v v2, (a0)

vl4r.v v4, (a0)  # Pseudo instruction equal to vl4re8.v
vl4re8.v v4, (a0)  # Load v4-v7 with 4*VLEN/8 bytes from address in a0
vl4re16.v v4, (a0)
vl4re32.v v4, (a0)
vl4re64.v v4, (a0)
vl4re128.v v4, (a0)
vl4re256.v v4, (a0)
vl4re512.v v4, (a0)
vl4re1024.v v4, (a0)

vl8r.v v8, (a0)  # Pseudo instruction equal to vl8re8.v
vl8re8.v v8, (a0)  # Load v8-v15 with 8*VLEN/8 bytes from address in a0
vl8re16.v v8, (a0)
vl8re32.v v8, (a0)
vl8re64.v v8, (a0)
vl8re128.v v8, (a0)
vl8re256.v v8, (a0)
vl8re512.v v8, (a0)
vl8re1024.v v8, (a0)

vs1r.v v3, (a1)  # Store v3 to address in a1
vs2r.v v2, (a1)  # Store v2-v3 to address in a1
vs4r.v v4, (a1)  # Store v4-v7 to address in a1
vs8r.v v8, (a1)  # Store v8-v15 to address in a1

Note: Implementations should raise illegal instruction exceptions on vl<nf>r instructions for EEW values that are not supported.

Note: These instructions can be implemented as unit-stride loads/stores of vector register groups, where EEW is 8, nf encodes EMUL, and vl = VLMAX for EEW and EMUL.

Note: We have considered adding a whole register mask load instruction (vl1re1.v vd, (rs1)), with EEW=1, as a mask hint but this is not currently on PoR.
8. Vector AMO Operations

This instruction subset is given the ISA string Zvamo.

Note: This set of instructions is included in the base "V" extension used for the Unix profile.

If vector AMO instructions are supported, then the scalar Zaamo instructions (atomic operations from the standard A extension) must be present.

Vector AMO operations are encoded using the unused width encodings under the standard AMO major opcode. Each active element performs an atomic read-modify-write of a single memory location.

Format for Vector AMO Instructions under AMO major opcode

```
<table>
<thead>
<tr>
<th>31</th>
<th>amoop</th>
<th>wd</th>
<th>vm</th>
<th>vs2/</th>
<th>rs1</th>
<th>width</th>
<th>vs3/vd</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
```

vs2[4:0] specifies v register holding address
vs3/vd[4:0] specifies v register holding source operand and destination

vm specifies vector mask

width[2:0] specifies size of index elements, and distinguishes from scalar AMO
amoop[4:0] specifies the AMO operation

wd specifies whether the original memory value is written to vd (1=yes, 0=no)

The vs2 vector register supplies the byte offset of each element, while the vs3 vector register supplies the source data for the atomic memory operation.

AMOs have the same index EEW scheme as indexed operations, except without the mew bit, which is required to be zero, so offsets can have EEW=8,16,32,64 only. A vector of byte offsets in register vs2 is added to the scalar base register in rs1 to give the addresses of the AMO operations.

The data register vs3 used the dynamic SEW and LMUL settings in vtype.

If the wd bit is set, the vd register is written with the initial value of the memory element. If the wd bit is clear, the vd register is not written.

Note: When wd is clear, the memory system does not need to return the original memory value, and the original values in vd will be preserved.

The AMOs were defined to overwrite source data partly to reduce total memory pipeline read port count for implementations with register renaming. Also to support the same addressing mode as vector indexed operations, and because vector AMOs are less likely to need results given that the primary use is parallel in-memory reductions.

Vector AMOs operate as if aq and rl bits were zero on each element with regard to ordering relative to other instructions in the same hart.

Vector AMOs provide no ordering guarantee between element operations in the same vector AMO instruction.

<table>
<thead>
<tr>
<th>Width [2:0]</th>
<th>Index EEW</th>
<th>Mem data bits</th>
<th>Reg data bits</th>
<th>Opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard scalar AMO</td>
<td>0 1 0</td>
<td>-</td>
<td>32</td>
<td>XLEN</td>
</tr>
<tr>
<td>Standard scalar AMO</td>
<td>0 1 1</td>
<td>-</td>
<td>64</td>
<td>XLEN</td>
</tr>
<tr>
<td>Standard scalar AMO</td>
<td>1 0 0</td>
<td>-</td>
<td>128</td>
<td>XLEN</td>
</tr>
<tr>
<td>Vector AMO</td>
<td>0 0 0</td>
<td>8</td>
<td>SEW</td>
<td>SEW</td>
</tr>
<tr>
<td>Vector AMO</td>
<td>1 0 1</td>
<td>16</td>
<td>SEW</td>
<td>SEW</td>
</tr>
<tr>
<td>Vector AMO</td>
<td>1 1 0</td>
<td>32</td>
<td>SEW</td>
<td>SEW</td>
</tr>
<tr>
<td>Vector AMO</td>
<td>1 1 1</td>
<td>64</td>
<td>SEW</td>
<td>SEW</td>
</tr>
</tbody>
</table>
Index bits is the EEW of the offsets.

Mem bits is the size of element accessed in memory

Reg bits is the size of element accessed in register

If index EEW is less than XLEN, then addresses in the vector vs2 are zero-extended to XLEN. If index EEW is greater than XLEN, the instruction encoding is reserved.

Vector AMO instructions are only supported for the memory data element widths (in SEW) supported by AMOs in the implementation’s scalar architecture. Other element width encodings are reserved.

The vector amoop[4:0] field uses the same encoding as the scalar 5-bit AMO instruction field, except that LR and SC are not supported.

<table>
<thead>
<tr>
<th>amoop</th>
<th>opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 1</td>
<td>vamoswap</td>
</tr>
<tr>
<td>0 0 0 0 0</td>
<td>vamoadd</td>
</tr>
<tr>
<td>0 0 1 0 0</td>
<td>vamoxor</td>
</tr>
<tr>
<td>0 1 1 0 0</td>
<td>vamoand</td>
</tr>
<tr>
<td>0 1 0 0 0</td>
<td>vamoor</td>
</tr>
<tr>
<td>1 0 0 0 0</td>
<td>vamomin</td>
</tr>
<tr>
<td>1 0 1 0 0</td>
<td>vamomax</td>
</tr>
<tr>
<td>1 1 0 0 0</td>
<td>vamominu</td>
</tr>
<tr>
<td>1 1 1 0 0</td>
<td>vamomaxu</td>
</tr>
</tbody>
</table>

The assembly syntax uses x0 in the destination register position to indicate the return value is not required (wd=0).
# Vector AMOs for index EEW=8
vamoswapei8.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoswapei8.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoaddei8.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoaddei8.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoxorei8.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoxorei8.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoannde18.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoannde18.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoorei8.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoorei8.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamominei8.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamominei8.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamomaxei8.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamomaxei8.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamominuei8.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamominuei8.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamomaxuei8.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamomaxuei8.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0

# Vector AMOs for index EEW=16
vamoswapei16.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoswapei16.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoaddei16.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoaddei16.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoxorei16.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoxorei16.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoannde16.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoannde16.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoorei16.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoorei16.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamominei16.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamominei16.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamomaxei16.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamomaxei16.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamominuei16.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamominuei16.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamomaxuei16.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamomaxuei16.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0

# Vector AMOs for index EEW=32
vamoswapei32.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoswapei32.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoaddei32.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoaddei32.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoxorei32.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoxorei32.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoandei32.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoandei32.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoorei32.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoorei32.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamominei32.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamominei32.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamomaxei32.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamomaxei32.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamominuei32.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamominuei32.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamomaxuei32.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamomaxuei32.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0

# Vector AMOs for index EEW=64
vamoswapei64.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoswapei64.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoaddei64.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoaddei64.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoxorei64.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoxorei64.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoandei64.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoandei64.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamoorei64.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamoorei64.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamominei64.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamominei64.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamomaxei64.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamomaxei64.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamominuei64.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamominuei64.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
vamomaxuei64.v vd, (rs1), vs2, vd, v0.t # Write original value to register, wd=1
vamomaxuei64.v x0, (rs1), vs2, vs3, v0.t # Do not write original value to register, wd=0
9. Vector Memory Alignment Constraints

If an element accessed by a vector memory instruction is not naturally aligned to the size of the element, either the element is transferred successfully or an address misaligned exception is raised on that element.

Support for misaligned vector memory accesses is independent of an implementation’s support for misaligned scalar memory accesses.

Note: An implementation may have neither, one, or both scalar and vector memory accesses support some or all misaligned accesses in hardware. A separate PMA should be defined to determine if vector misaligned accesses are supported in the associated address range.

Vector misaligned memory accesses follow the same rules for atomicity as scalar misaligned memory accesses.
Vector memory instructions appear to execute in program order on the local hart. Vector memory instructions follow RVWMO at the instruction level, and element operations are ordered within the instruction as if performed by an element-ordered sequence of syntactically independent scalar instructions. Vector indexed-ordered loads and stores read and write elements from/to memory in element order respectively. Vector indexed-unordered loads and stores do not preserve element order for reads and writes within a single vector load or store instruction respectively.

Note: More formal definitions required.
11. Vector Arithmetic Instruction Formats

The vector arithmetic instructions use a new major opcode (OP-V = 1010111) which neighbors OP-FP. The three-bit funct3 field is used to define sub-categories of vector instructions.

Formats for Vector Arithmetic Instructions under OP-V major opcode

### 11.1. Vector Arithmetic Instruction encoding

The funct3 field encodes the operand type and source locations.

<table>
<thead>
<tr>
<th>funct3[2:0]</th>
<th>Category</th>
<th>Operands</th>
<th>Type of scalar operand</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>OPIVV</td>
<td>vector-vector</td>
<td>N/A</td>
</tr>
<tr>
<td>0 0 1</td>
<td>OPFVV</td>
<td>vector-vector</td>
<td>N/A</td>
</tr>
<tr>
<td>0 1 0</td>
<td>OPMVV</td>
<td>vector-vector</td>
<td>N/A</td>
</tr>
<tr>
<td>0 1 1</td>
<td>OPIVI</td>
<td>vector-immediate</td>
<td>imm[4:0]</td>
</tr>
<tr>
<td>1 0 0</td>
<td>OPIVX</td>
<td>vector-scalar</td>
<td>GPR x register rs1</td>
</tr>
<tr>
<td>1 0 1</td>
<td>OPFVF</td>
<td>vector-scalar</td>
<td>FP f register rs1</td>
</tr>
<tr>
<td>1 1 0</td>
<td>OPMVX</td>
<td>vector-scalar</td>
<td>GPR x register rs1</td>
</tr>
<tr>
<td>1 1 1</td>
<td>OPCFG</td>
<td>scalars-imms</td>
<td>GPR x register rs1 &amp; rs2/imm</td>
</tr>
</tbody>
</table>

Integer operations are performed using unsigned or two's-complement signed integer arithmetic depending on the opcode.

Note: In this discussion, fixed-point operations are considered to be integer operations.

All standard vector floating-point arithmetic operations follow the IEEE-754/2008 standard. All vector floating-point operations use the dynamic rounding mode in the frm register. Use of the frm field when it contains an invalid rounding mode by any vector floating-point instruction, even those that do not depend on the rounding mode, or when vl=0, or when vstart ≥ vl, is reserved.

Note: All vector floating-point code will rely on a valid value in frm. Implementations can make all vector FP instructions report exceptions when the rounding mode is invalid to simplify control logic.

Vector-vector operations take two vectors of operands from vector register groups specified by vs2 and vs1 respectively.

Vector-scalar operations can have three possible forms, but in all cases take one vector of operands from a vector register group specified by vs2 and a second scalar source operand from one of three alternative sources.
1. For integer operations, the scalar can be a 5-bit immediate encoded in the \texttt{rs1} field. The value is sign-extended to SEW bits, unless otherwise specified. For integer operations, the scalar can be taken from the scalar \texttt{x} register specified by \texttt{rs1}. If XLEN>SEW, the least-significant SEW bits of the \texttt{x} register are used, unless otherwise specified. If XLEN<SEW, the value from the \texttt{x} register is sign-extended to SEW bits. For floating-point operations, the scalar can be taken from a scalar \texttt{f} register. If FLEN > SEW, the value in the \texttt{f} registers is checked for a valid NaN-boxed value, in which case the least-significant SEW bits of the \texttt{f} register are used, else the canonical NaN value is used. Vector instructions where any floating-point vector operand’s EEW is not a supported floating-point type width (which includes when FLEN < SEW) are reserved.

Note Some instructions zero-extend the 5-bit immediate, and denote this by naming the immediate \texttt{uimm} in the assembly syntax.

Note The proposed Zfinx variants will take the floating-point scalar argument from the \texttt{x} registers.

Vector arithmetic instructions are masked under control of the \texttt{vm} field.

\begin{verbatim}
# Assembly syntax pattern for vector binary arithmetic instructions

# Operations returning vector results, masked by vm (v8.t, <nothing>)
vop.vv  vd, vs2, vs1, vm  # integer vector-vector      vd[i] = vs2[i] op vs1[i]
vop.vx  vd, vs2, rs1, vm  # integer vector-scalar      vd[i] = vs2[i] op x[rs1]
vop.vi  vd, vs2, imm, vm  # integer vector-immediate   vd[i] = vs2[i] op imm

vfop.vv vd, vs2, vs1, vm  # FP vector-vector operation vd[i] = vs2[i] fop vs1[i]
vfop.vf vd, vs2, rs1, vm  # FP vector-scalar operation vd[i] = vs2[i] fop f[rs1]

# Assembly syntax pattern for vector ternary arithmetic instructions (multiply-add)

# Integer operations overwriting sum input
vop.vv vd, vs1, vs2, vm  # vd[i] = vs1[i] * vs2[i] + vd[i]
vop.vx vd, rs1, vs2, vm  # vd[i] = x[rs1] * vs2[i] + vd[i]

# Integer operations overwriting product input
vop.vv vd, vs1, vs2, vm  # vd[i] = vs1[i] * vd[i] + vs2[i]
vop.vx vd, rs1, vs2, vm  # vd[i] = x[rs1] * vd[i] + vs2[i]

# Floating-point operations overwriting sum input
vfop.vv vd, vs1, vs2, vm  # vd[i] = vs1[i] * vs2[i] + vd[i]
vfop.vf vd, rs1, vs2, vm  # vd[i] = f[rs1] * vs2[i] + vd[i]

# Floating-point operations overwriting product input
vfop.vv vd, vs1, vs2, vm  # vd[i] = vs1[i] * vd[i] + vs2[i]
vfop.vf vd, rs1, vs2, vm  # vd[i] = f[rs1] * vd[i] + vs2[i]

Note For ternary multiply-add operations, the assembler syntax always places the destination vector register first, followed by either \texttt{rs1} or \texttt{vs1}, then \texttt{vs2}. This ordering provides a more natural reading of the assembler for these ternary operations, as the multiply operands are always next to each other.

11.2. Widening Vector Arithmetic Instructions

A few vector arithmetic instructions are defined to be \textit{widening} operations where the destination vector register group has EEW=2*SEW and EMUL=2*LMUL.

The first vector register group operand can be either single or double-width. These are generally written with a \texttt{vw*} prefix on the opcode or \texttt{vfw*} for vector floating-point operations.
Assembly syntax pattern for vector widening arithmetic instructions

# Double-width result, two single-width sources: 2*SEW = SEW op SEW
vwop.vv vd, vs2, vs1, vm # integer vector-vector      vd[i] = vs2[i] op vs1[i]
vwop.vx vd, vs2, rs1, vm  # integer vector-scalar      vd[i] = vs2[i] op x[rs1]

# Double-width result, first source double-width, second source single-width: 2*SEW = 2*SEW op SEW
vwop.wv vd, vs2, vs1, vm  # integer vector-vector      vd[i] = vs2[i] op vs1[i]
vwop.wx vd, vs2, rs1, vm  # integer vector-scalar      vd[i] = vs2[i] op x[rs1]

Note: Originally, a w suffix was used on opcode, but this could be confused with the use of a w suffix to mean word-sized operations in doubleword integers, so the w was moved to prefix.

Note: The floating-point widening operations were changed to vfw* from vwf* to be more consistent with any scalar widening floating-point operations that will be written as fw*.

Note: For integer multiply-add, another possible widening option increases the size of the accumulator to EEW=4*SEW (i.e., 4*SEW += SEW*SEW). These would be distinguished by a vq* prefix on the opcode, for quad-widening. These are not included at this time, but are a possible addition in a future extension.

For all widening instructions, the destination EEW and EMUL values must be a supported configuration, otherwise the instruction encoding is reserved.

The destination vector register group must be specified using a vector register number that is valid for the destination's EMUL, otherwise the instruction encoding is reserved.

Note: This constraint is necessary to support restart with non-zero vstart.

Note: For the vw<op>.wv vd, vs2, vs1 format instructions, it is legal for vd to equal vs2.

11.3. Narrowing Vector Arithmetic Instructions

A few instructions are provided to convert double-width source vectors into single-width destination vectors. These instructions convert a vector register group with EEW/EMUL=2*SEW/2*LMUL to a vector register group with the current SEW/LMUL setting.

If EEW > ELEN or EMUL > 8, the instruction encoding is reserved.

Note: An alternative design decision would have been to treat SEW/LMUL as defining the size of the source vector register group. The choice here is motivated by the belief the chosen approach will require fewer vtype changes.

The source and destination vector register groups have to be specified with a vector register number that is legal for the source and destination EMUL values respectively, otherwise the instruction encoding is reserved.

Where there is a second source vector register group (specified by vs1), this has the same (narrower) width as the result (i.e., EEW=SEW).

Note: It is safe to overwrite a second source vector register group with the same EEW and EMUL as the result.

A vn* prefix on the opcode is used to distinguish these instructions in the assembler, or a vfn* prefix for narrowing floating-point opcodes. The double-width source vector register group is signified by a w in the source operand suffix (e.g., vnsra.wv)

Note: Comparison operations that set a mask register are also implicitly a narrowing operation.
12. Vector Integer Arithmetic Instructions

A set of vector integer arithmetic instructions is provided.

12.1. Vector Single-Width Integer Add and Subtract

Vector integer add and subtract are provided. Reverse-subtract instructions are also provided for the vector-scalar forms.

```
# Integer adds.
vadd.vv vd, vs2, vs1, vm   # Vector-vector
vadd.vx vd, vs2, rs1, vm   # vector-scalar
vadd.vi vd, vs2, imm, vm   # vector-immediate

# Integer subtract
vsub.vv vd, vs2, vs1, vm   # Vector-vector
vsub.vx vd, vs2, rs1, vm   # vector-scalar

# Integer reverse subtract
vrsub.vx vd, vs2, rs1, vm   # vd[i] = rs1 - vs2[i]
vrsub.vi vd, vs2, imm, vm   # vd[i] = imm - vs2[i]
```

Note: A vector of integer values can be negated using a reverse-subtract instruction with a scalar operand of x0. Can define assembly pseudoinstruction `vneg.v vd,vs = vrsub.vx vd,vs,x0`.

12.2. Vector Widening Integer Add/Subtract

The widening add/subtract instructions are provided in both signed and unsigned variants, depending on whether the narrower source operands are first sign- or zero-extended before forming the double-width sum.

```
# Widening unsigned integer add/subtract, 2*SEW = SEW +/- SEW
vwaddu.vv vd, vs2, vs1, vm   # vector-vector
vwaddu.vx vd, vs2, rs1, vm   # vector-scalar
vwsubu.vv vd, vs2, vs1, vm   # vector-vector
vwsubu.vx vd, vs2, rs1, vm   # vector-scalar

# Widening signed integer add/subtract, 2*SEW = SEW +/- SEW
vwadd.vv vd, vs2, vs1, vm   # vector-vector
vwadd.vx vd, vs2, rs1, vm   # vector-scalar
vwsub.vv vd, vs2, vs1, vm   # vector-vector
vwsub.vx vd, vs2, rs1, vm   # vector-scalar

# Widening unsigned integer add/subtract, 2*SEW = 2*SEW +/- SEW
vwaddu.wv vd, vs2, vs1, vm   # vector-vector
vwaddu.wx vd, vs2, rs1, vm   # vector-scalar
vwsubu.wv vd, vs2, vs1, vm   # vector-vector
vwsubu.wx vd, vs2, rs1, vm   # vector-scalar

# Widening signed integer add/subtract, 2*SEW = 2*SEW +/- SEW
vwadd.wv vd, vs2, vs1, vm   # vector-vector
vwadd.wx vd, vs2, rs1, vm   # vector-scalar
vwsub.wv vd, vs2, vs1, vm   # vector-vector
vwsub.wx vd, vs2, rs1, vm   # vector-scalar
```

Note: An integer value can be doubled in width using the widening add instructions with a scalar operand of x0. Can define assembly pseudoinstructions `vwcvt.x.x.v vd,vs,vm = vwadd.vx vd,vs,x0,vm` and `vwcvtu.x.x.v vd,vs,vm = vwaddu.vx vd,vs,x0,vm`.

12.3. Vector Integer Extension
The vector integer extension instructions zero- or sign-extend a source vector integer operand with EEW less than SEW to fill SEW-sized elements in the destination. The EEW of the source is 1/2, 1/4, or 1/8 of SEW, while EMUL of the source is (EEW/SEW)*LMUL. The destination has EEW equal to SEW and EMUL equal to LMUL.

\[
\begin{align*}
vzext.vf2 & \ vd,\ vs2,\ vm \ # \ Zero-extend \ SEW/2 \ source \ to \ SEW \ destination \\
vsext.vf2 & \ vd,\ vs2,\ vm \ # \ Sign-extend \ SEW/2 \ source \ to \ SEW \ destination \\
vzext.vf4 & \ vd,\ vs2,\ vm \ # \ Zero-extend \ SEW/4 \ source \ to \ SEW \ destination \\
vsext.vf4 & \ vd,\ vs2,\ vm \ # \ Sign-extend \ SEW/4 \ source \ to \ SEW \ destination \\
vzext.vf8 & \ vd,\ vs2,\ vm \ # \ Zero-extend \ SEW/8 \ source \ to \ SEW \ destination \\
vsext.vf8 & \ vd,\ vs2,\ vm \ # \ Sign-extend \ SEW/8 \ source \ to \ SEW \ destination \\
\end{align*}
\]

If the source EEW is not a supported width, or source EMUL would be below the minimum legal LMUL, the instruction encoding is reserved.

### 12.4. Vector Integer Add-with-Carry / Subtract-with-Borrow Instructions

To support multi-word integer arithmetic, instructions that operate on a carry bit are provided. For each operation (add or subtract), two instructions are provided: one to provide the result (SEW width), and the second to generate the carry output (single bit encoded as a mask boolean).

The carry inputs and outputs are represented using the mask register layout as described in Section Mask Register Layout. Due to encoding constraints, the carry input must come from the implicit v0 register, but carry outputs can be written to any vector register that respects the source/destination overlap restrictions.

vadc and vsbc add or subtract the source operands and the carry-in or borrow-in, and write the result to vector register vd. These instructions are encoded as masked instructions (vm=0), but they operate on and write back all body elements. Encodings corresponding to the unmasked versions (vm=1) are reserved.

vmadc and vmsbc add or subtract the source operands, optionally add the carry-in or subtract the borrow-in if masked (vm=0), and write the result back to mask register vd. If unmasked (vm=1), there is no carry-in or borrow-in. These instructions operate on and write back all body elements, even if masked. Because these instructions produce a mask value, they always operate with a tail-agnostic policy.
# Produce sum with carry.

```assembly
# vd[i] = vs2[i] + vs1[i] + v0.mask[i]
vadc.vvm   vd, vs2, vs1, v0  # Vector-vector

# vd[i] = vs2[i] + x[rs1] + v0.mask[i]
vadc.vxm   vd, vs2, rs1, v0  # Vector-scalar

# vd[i] = vs2[i] + imm + v0.mask[i]
vadc.vim   vd, vs2, imm, v0  # Vector-immediate
```

# Produce carry out in mask register format

```assembly
# vd.mask[i] = carry_out(vs2[i] + vs1[i] + v0.mask[i])
vmadc.vvm   vd, vs2, vs1, v0  # Vector-vector

# vd.mask[i] = carry_out(vs2[i] + x[rs1] + v0.mask[i])
vmadc.vxm   vd, vs2, rs1, v0  # Vector-scalar

# vd.mask[i] = carry_out(vs2[i] + imm + v0.mask[i])
vmadc.vim   vd, vs2, imm, v0  # Vector-immediate

# vd.mask[i] = carry_out(vs2[i] + vs1[i])
vmadc.vv    vd, vs2, vs1  # Vector-vector, no carry-in

# vd.mask[i] = carry_out(vs2[i] + x[rs1])
vmadc.vx    vd, vs2, rs1  # Vector-scalar, no carry-in

# vd.mask[i] = carry_out(vs2[i] + imm)
vmadc.vi    vd, vs2, imm  # Vector-immediate, no carry-in
```

Because implementing a carry propagation requires executing two instructions with unchanged inputs, destructive accumulations will require an additional move to obtain correct results.

```assembly
# Example multi-word arithmetic sequence, accumulating into v4
vmadc.vvm v1, v4, v8, v0  # Get carry into temp register v1
vadc.vvm v4, v4, v8, v0  # Calc new sum
vmmv.m v0, v1       # Move temp carry into v0 for next word
```

The subtract with borrow instruction vsbc performs the equivalent function to support long word arithmetic for subtraction. There are no subtract with immediate instructions.
# Produce difference with borrow.

# vd[i] = vs2[i] - vs1[i] - v0.mask[i]
vsbc.vvm   vd, vs2, vs1, v0  # Vector-vector

# vd[i] = vs2[i] - x[rs1] - v0.mask[i]
vsbc.vxm   vd, vs2, rs1, v0  # Vector-scalar

# Produce borrow out in mask register format

# vd.mask[i] = borrow_out(vs2[i] - vs1[i] - v0.mask[i])
vmsbc.vvm   vd, vs2, vs1, v0  # Vector-vector

# vd.mask[i] = borrow_out(vs2[i] - x[rs1] - v0.mask[i])
vmsbc.vxm   vd, vs2, rs1, v0  # Vector-scalar

# vd.mask[i] = borrow_out(vs2[i] - vs1[i])
vmsbc.vv    vd, vs2, vs1      # Vector-vector, no borrow-in

# vd.mask[i] = borrow_out(vs2[i] - x[rs1])
vmsbc.vx    vd, vs2, rs1      # Vector-scalar, no borrow-in

For vmsbc, the borrow is defined to be 1 iff the difference, prior to truncation, is negative.

For vadc and vsbc, the instruction encoding is reserved if the destination vector register is v0.

Note: This constraint corresponds to the constraint on masked vector operations that overwrite the mask register.

12.5. Vector Bitwise Logical Instructions

# Bitwise logical operations.

vand.vv vd, vs2, vs1, vm   # Vector-vector
vand.vx vd, vs2, rs1, vm   # vector-scalar
vand.vi vd, vs2, imm, vm   # vector-immediate

vor.vv vd, vs2, vs1, vm   # Vector-vector
vor.vx vd, vs2, rs1, vm   # vector-scalar
vor.vi vd, vs2, imm, vm   # vector-immediate

vxor.vv vd, vs2, vs1, vm   # Vector-vector
vxor.vx vd, vs2, rs1, vm   # vector-scalar
vxor.vi vd, vs2, imm, vm   # vector-immediate

Note: With an immediate of -1, scalar-immediate forms of the vxor instruction provide a bitwise NOT operation. This can be provided as an assembler pseudoinstruction vnot.v.

12.6. Vector Single-Width Bit Shift Instructions

A full complement of vector shift instructions are provided, including logical shift left, and logical (zero-extending) and arithmetic (sign-extending) shift right.
# Bit shift operations

```
vsll.vv vd, vs2, vs1, vm  # Vector-vector
vsll.vx vd, vs2, rs1, vm  # vector-scalar
vsll.vi vd, vs2, uimm, vm  # vector-immediate

vsrl.vv vd, vs2, vs1, vm  # Vector-vector
vsrl.vx vd, vs2, rs1, vm  # vector-scalar
vsrl.vi vd, vs2, uimm, vm  # vector-immediate

vsra.vv vd, vs2, vs1, vm  # Vector-vector
vsra.vx vd, vs2, rs1, vm  # vector-scalar
vsra.vi vd, vs2, uimm, vm  # vector-immediate
```

The low \log_2(\text{SEW})\ bits of the vector or scalar shift-amount value are used, and shift-amount immediates are zero-extended.

## 12.7. Vector Narrowing Integer Right Shift Instructions

The narrowing right shifts extract a smaller field from a wider operand and have both zero-extending (srl) and sign-extending (sra) forms. The shift amount can come from a vector or a scalar register or a 5-bit immediate. The low \log_2(2*\text{SEW})\ bits of the vector or scalar shift-amount value are used (e.g., the low 6 bits for a SEW=64-bit to SEW=32-bit narrowing operation). The immediate forms zero-extend their shift-amount immediate operand.

```
# Narrowing shift right logical, SEW = (2*SEW) >> SEW
vnsrl.wv vd, vs2, vs1, vm  # vector-vector
vnsrl.wx vd, vs2, rs1, vm  # vector-scalar
vnsrl.wi vd, vs2, uimm, vm  # vector-immediate

# Narrowing shift right arithmetic, SEW = (2*SEW) >> SEW
vnsra.wv vd, vs2, vs1, vm  # vector-vector
vnsra.wx vd, vs2, rs1, vm  # vector-scalar
vnsra.wi vd, vs2, uimm, vm  # vector-immediate
```

**Note**

It could be useful to add support for n4 variants, where the destination is 1/4 width of source.

**Note**

An integer value can be halved in width using the narrowing integer shift instructions with a scalar operand of x0. Can define assembly pseudoinstructions `vncvt.x.x.w vd,vs,vm = vnsrl.wx vd,vs,x0,vm`.

## 12.8. Vector Integer Comparison Instructions

The following integer compare instructions write 1 to the destination mask register element if the comparison evaluates to true, and 0 otherwise. The destination mask vector is always held in a single vector register, with a layout of elements as described in Section Mask Register Layout. The destination mask vector register may be the same as the source vector mask register (v0).
The following table indicates how all comparisons are implemented in native machine code.
<table>
<thead>
<tr>
<th>Comparison</th>
<th>Assembler Mapping</th>
<th>Assembler Pseudoinstruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>va &lt; vb</td>
<td>vmslt{u}.vv vd, va, vb, vm</td>
<td></td>
</tr>
<tr>
<td>va &lt;= vb</td>
<td>vmsle{u}.vv vd, va, vb, vm</td>
<td>vmsgt{u}.vv vd, va, vb, vm</td>
</tr>
<tr>
<td>va &gt; vb</td>
<td>vmslt{u}.vv vd, vb, va, vm</td>
<td></td>
</tr>
<tr>
<td>va &gt;= vb</td>
<td>vmsle{u}.vv vd, vb, va, vm</td>
<td>vmsgt{u}.vv vd, va, vb, vm</td>
</tr>
<tr>
<td>va &lt; x</td>
<td>vmslt{u}.vx vd, va, x, vm</td>
<td></td>
</tr>
<tr>
<td>va &lt;= x</td>
<td>vmsle{u}.vx vd, va, x, vm</td>
<td></td>
</tr>
<tr>
<td>va &gt; x</td>
<td>vmsgt{u}.vx vd, va, x, vm</td>
<td></td>
</tr>
<tr>
<td>va &gt;= x</td>
<td>see below</td>
<td></td>
</tr>
</tbody>
</table>

va, vb vector register groups

x  scalar integer register

i  immediate

Note

The immediate forms of vmslt{u}.vi are not provided as the immediate value can be decreased by 1 and the vmsle{u}.vi variants used instead. The vmsle.vi range is -16 to 15, resulting in an effective vmslt.vi range of -15 to 16. The vmsle.u.vi range is 0 to 15 giving an effective vmslt.u.vi range of 1 to 16 (Note, vmsltu.vi with immediate 0 is not useful as it is always false). Because the 5-bit vector immediates are always sign-extended, vmsleu.vi also supports unsigned immediate values in the range 2^{SEW-16} to 2^{SEW-1}, allowing corresponding vmsltu.vi comparisons against unsigned immediates in the range 2^{SEW-15} to 2^{SEW}. Note that vlsltu.vi with immediate 2^{SEW} is not useful as it is always true.

Similarly, vmsge{u}.vi is not provided and the comparison is implemented using vmsgt{u}.vi with the immediate decremented by one. The resulting effective vmsg.e.vi range is -15 to 16, and the resulting effective vmsgeu.vi range is 1 to 16 (Note, vmsgeu.vi with immediate 0 is not useful as it is always true).

Note

The vmsgt forms for register scalar and immediates are provided to allow a single comparison instruction to provide the correct polarity of mask value without using additional mask logical instructions.

To reduce encoding space, the vmsge{u}.vx form is not directly provided, and so the va ≥ x case requires special treatment.

Note

The vmsge(u).vx could potentially be encoded in a non-orthogonal way under the unused OPIVI variant of vmslt{u}. These would be the only instructions in OPIVI that use a scalar ‘x’ register however. Alternatively, a further two funct6 encodings could be used, but these would have a different operand format (writes to mask register) than others in the same group of 8 funct6 encodings. The current PoR is to omit these instructions and to synthesize where needed as described below.

The vmsge{u}.vx operation can be synthesized by reducing the value of x by 1 and using the vmsgt{u}.vx instruction, when it is known that this will not underflow the representation in x.

Sequences to synthesize ‘vmsge{u}.vx’ instruction

va >= x,  x > minimum

addi t0, x, -1; vmsgt{u}.vx vd, va, t0, vm

The above sequence will usually be the most efficient implementation, but assembler pseudoinstructions can be provided for cases where the range of x is unknown.
unmasked va >= x

pseudoinstruction: vmsge{u}.vx vd, va, x
expansion: vmslt{u}.vx vd, va, x; vmnand.mm vd, vd, vd

masked va >= x, vd != v0

pseudoinstruction: vmsge{u}.vx vd, va, x, v0.t
expansion: vmslt{u}.vx vd, va, x, v0.t; vmxor.mm vd, vd, v0

masked va >= x, vd == v0

pseudoinstruction: vmsge{u}.vx vd, va, x, v0.t, vt
expansion: vmslt{u}.vx vt, va, x; vmandnot.mm vd, vd, vt

masked va >= x, any vd

pseudoinstruction: vmsge{u}.vx vd, va, x, v0.t, vt
expansion: vmslt{u}.vx vt, va, x; vmandnot.mm vt, v0, vt; vmandnot.mm vd, vd, v0; vmor.mm vd, vt,

The vt argument to the pseudoinstruction must name a temporary vector register that is not same as vd and which will be clobbered by the pseudoinstruction

Comparisons effectively AND in the mask under a mask-undisturbed policy e.g.

# (a < b) && (b < c) in two instructions when mask-undisturbed
vmslt.vv v0, va, vb        # All body elements written
vmslt.vv v0, vb, vc, v0.t   # Only update at set mask

Comparisons write mask registers, and so always operate under a tail-agnostic policy.

12.9. Vector Integer Min/Max Instructions

Signed and unsigned integer minimum and maximum instructions are supported.

# Unsigned minimum
vminu.vv vd, vs2, vs1, vm   # Vector-vector
vminu.vx vd, vs2, rs1, vm   # vector-scalar

# Signed minimum
vmin.vv vd, vs2, vs1, vm    # Vector-vector
vmin.vx vd, vs2, rs1, vm    # vector-scalar

# Unsigned maximum
vmaxu.vv vd, vs2, vs1, vm   # Vector-vector
vmaxu.vx vd, vs2, rs1, vm   # vector-scalar

# Signed maximum
vmax.vv vd, vs2, vs1, vm    # Vector-vector
vmax.vx vd, vs2, rs1, vm    # vector-scalar

12.10. Vector Single-Width Integer Multiply Instructions

The single-width multiply instructions perform a SEW-bit*SEW-bit multiply and return an SEW-bit-wide result. The mulh versions write the high word of the product to the destination register.
# Signed multiply, returning low bits of product
vmul.vv vd, vs2, vs1, vm   # Vector-vector
vmul.vx vd, vs2, vs1, vm   # vector-scalar

# Signed multiply, returning high bits of product
vmulh.vv vd, vs2, vs1, vm  # Vector-vector
vmulh.vx vd, vs2, vs1, vm  # vector-scalar

# Unsigned multiply, returning high bits of product
vmulhu.vv vd, vs2, vs1, vm  # Vector-vector
vmulhu.vx vd, vs2, vs1, vm  # vector-scalar

# Signed(vs2)-Unsigned multiply, returning high bits of product
vmulhsu.vv vd, vs2, vs1, vm  # Vector-vector
vmulhsu.vx vd, vs2, vs1, vm  # vector-scalar

**Note**
There is no vmulhus opcode to return high half of unsigned-vector * signed-scalar product.

The current vmulh* opcodes perform simple fractional multiplies, but with no option to scale, round, and/or saturate the result. A possible extension can consider variants of vmulh, vmulhu, vmulhusu that use the vxrm rounding mode when discarding low half of product. There is no possibility of overflow in these cases.

### 12.11. Vector Integer Divide Instructions

The divide and remainder instructions are equivalent to the RISC-V standard scalar integer multiply/divides, with the same results for extreme inputs.

# Unsigned divide.
vdivu.vv vd, vs2, vs1, vm   # Vector-vector
vdivu.vx vd, vs2, vs1, vm   # vector-scalar

# Signed divide
vdiv.vv vd, vs2, vs1, vm   # Vector-vector
vdiv.vx vd, vs2, vs1, vm   # vector-scalar

# Unsigned remainder
vremu.vv vd, vs2, vs1, vm   # Vector-vector
vremu.vx vd, vs2, vs1, vm   # vector-scalar

# Signed remainder
vrem.vv vd, vs2, vs1, vm   # Vector-vector
vrem.vx vd, vs2, vs1, vm   # vector-scalar

**Note**
The decision to include integer divide and remainder was contentious. The argument in favor is that without a standard instruction, software would have to pick some algorithm to perform the operation, which would likely perform poorly on some microarchitectures versus others.

**Note**
There is no instruction to perform a "scalar divide by vector" operation.

### 12.12. Vector Widening Integer Multiply Instructions

The widening integer multiply instructions return the full 2*SEW-bit product from an SEW-bit*SEW-bit multiply.
12.13. Vector Single-Width Integer Multiply-Add Instructions

The integer multiply-add instructions are destructive and are provided in two forms, one that overwrites the addend or minuend (vmacc, vnmsac) and one that overwrites the first multiplicand (vmadd, vnmsub).

The low half of the product is added or subtracted from the third operand.

Note: \textit{sac} is intended to be read as "subtract from accumulator". The opcode is vnmsac to match the (unfortunately counterintuitive) floating-point fnmsub instruction definition. Similarly for the vnmsub opcode.


The widening integer multiply-add instructions add a SEW-bit*SEW-bit multiply result to (from) a 2*SEW-bit value and produce a 2*SEW-bit result. All combinations of signed and unsigned multiply operands are supported.

12.15. Vector Integer Merge Instructions
The vector integer merge instructions combine two source operands based on a mask. Unlike regular arithmetic instructions, the merge operates on all body elements (i.e., the set of elements from \(v_{\text{start}}\) up to the current vector length in \(v_l\)).

The \textit{vmerge} instructions are encoded as masked instruction (vm=0). The instructions combine two sources as follows. At elements where the mask value is zero, the first operand is copied to the destination element, otherwise the second operand is copied to the destination element. The first operand is always a vector register group specified by \(vs_2\). The second operand is a vector register group specified by \(vs_1\) or a scalar \(x\) register specified by \(rs_1\) or a 5-bit sign-extended immediate.

\[
\begin{align*}
\text{vmerge.vvm } vd, vs_2, vs_1, v0 & \ # vd[i] = v0.mask[i] ? vs_1[i] : vs_2[i] \\
\text{vmerge.vxm } vd, vs_2, rs_1, v0 & \ # vd[i] = v0.mask[i] ? x[rs_1] : vs_2[i] \\
\text{vmerge.vim } vd, vs_2, imm, v0 & \ # vd[i] = v0.mask[i] ? imm : vs_2[i]
\end{align*}
\]

12.16. Vector Integer Move Instructions

The vector integer move instructions copy a source operand to a vector register group. The \textit{vmv.v.v} variant copies a vector register group, whereas the \textit{vmv.v.x} and \textit{vmv.v.i} variants \textit{splat} a scalar register or immediate to all active elements of the destination vector register group. These instructions are encoded as unmasked instructions (vm=1). The first operand specifier (\(vs_2\)) must contain \(v_0\), and any other vector register number in \(vs_2\) is reserved.

\[
\begin{align*}
\text{vmv.v.v } vd, vs_1 & \ # vd[i] = vs_1[i] \\
\text{vmv.v.x } vd, rs_1 & \ # vd[i] = rs_1 \\
\text{vmv.v.i } vd, imm & \ # vd[i] = imm
\end{align*}
\]

\textbf{Note} Mask values can be widened into SEW-width elements using a sequence \textit{vmv.v.i } vd, 0; \textit{vmerge.vim } vd, vd, 1, v0.

The vector integer move instructions share the encoding with the vector merge instructions, but with \(vm=1\) and \(vs_2=v0\).

The form \textit{vmv.v.v } vd, \ vd, which leaves body elements unchanged, is used as a HINT to indicate that the register will next be used with an EEW equal to SEW.

\textbf{Note} Implementations that internally reorganize data according to EEW can shuffle the internal representation according to SEW. Implementations that do not internally reorganize data can dynamically elide this instruction, and treat as a NOP.
13. Vector Fixed-Point Arithmetic Instructions

The preceding set of integer arithmetic instructions is extended to support fixed-point arithmetic.

A fixed-point number is a two's-complement signed or unsigned integer interpreted as the numerator in a fraction with an implicit denominator. The fixed-point instructions are intended to be applied to the numerators; it is the responsibility of software to manage the denominators. An N-bit element can hold two's-complement signed integers in the range $-2^{N-1}$...$+2^{N-1}$-1, and unsigned integers in the range 0 ... $+2^{N-1}$. The fixed-point instructions help preserve precision in narrow operands by supporting scaling and rounding, and can handle overflow by saturating results into the destination format range.

Note: The widening integer operations described above can also be used to avoid overflow.

13.1. Vector Single-Width Saturating Add and Subtract

Saturating forms of integer add and subtract are provided, for both signed and unsigned integers. If the result would overflow the destination, the result is replaced with the closest representable value, and the vxsat bit is set.

```
# Saturating adds of unsigned integers.
vsaddu.vv vd, vs2, vs1, vm       # Vector-vector
vsaddu.vx vd, vs2, rs1, vm      # vector-scalar
vsaddu.vi vd, vs2, imm, vm      # vector-immediate

# Saturating adds of signed integers.
vsadd.vv vd, vs2, vs1, vm        # Vector-vector
vsadd.vx vd, vs2, rs1, vm        # vector-scalar
vsadd.vi vd, vs2, imm, vm        # vector-immediate

# Saturating subtract of unsigned integers.
vssubu.vv vd, vs2, vs1, vm       # Vector-vector
vssubu.vx vd, vs2, rs1, vm       # vector-scalar

# Saturating subtract of signed integers.
vssub.vv vd, vs2, vs1, vm         # Vector-vector
vssub.vx vd, vs2, rs1, vm         # vector-scalar
```

13.2. Vector Single-Width Averaging Add and Subtract

The averaging add and subtract instructions right shift the result by one bit and round off the result according to the setting in vxrm. Both unsigned and signed versions are provided. For vaaddu, vaadd, and vasub, there can be no overflow in the result. For vssubu, overflow is ignored and the result wraps around.
# Averaging add

# Averaging adds of unsigned integers.
vaaddu.vv vd, vs2, vs1, vm  # roundoff_unsigned(vs2[i] + vs1[i], 1)
vaaddu.vx vd, vs2, Rs1, vm  # roundoff_unsigned(vs2[i] + x[rs1], 1)

# Averaging adds of signed integers.
vaadd.vv vd, vs2, vs1, vm  # roundoff_signed(vs2[i] + vs1[i], 1)
vaadd.vx vd, vs2, Rs1, vm  # roundoff_signed(vs2[i] + x[rs1], 1)

# Averaging subtract

# Averaging subtract of unsigned integers.
vasubu.vv vd, vs2, vs1, vm  # roundoff_unsigned(vs2[i] - vs1[i], 1)
vasubu.vx vd, vs2, Rs1, vm  # roundoff_unsigned(vs2[i] - x[rs1], 1)

# Averaging subtract of signed integers.
vasub.vv vd, vs2, vs1, vm  # roundoff_signed(vs2[i] - vs1[i], 1)
vasub.vx vd, vs2, Rs1, vm  # roundoff_signed(vs2[i] - x[rs1], 1)

13.3. Vector Single-Width Fractional Multiply with Rounding and Saturation

The signed fractional multiply instruction produces a 2*SEW product of the two SEW inputs, then shifts the result right by SEW-1 bits, rounding these bits according to `vxrm`, then saturates the result to fit into SEW bits. If the result causes saturation, the `vxsat` bit is set.

# Signed saturating and rounding fractional multiply
# See vxrm description for rounding calculation
vsmul.vv vd, vs2, vs1, vm  # vd[i] = clip(roundoff_signed(vs2[i]*vs1[i], SEW-1))
vsmul.vx vd, vs2, Rs1, vm  # vd[i] = clip(roundoff_signed(vs2[i]*x[rs1], SEW-1))

Note: When multiplying two N-bit signed numbers, the largest magnitude is obtained for \(-2^{N-1} \cdot -2^{N-1}\) producing a result \(+2^{2N-2}\), which has a single (zero) sign bit when held in 2N bits. All other products have two sign bits in 2N bits. To retain greater precision in N result bits, the product is shifted right by one bit less than N, saturating the largest magnitude result but increasing result precision by one bit for all other products.

Note: We do not provide an equivalent fractional multiply where one input is unsigned, as these would retain all upper SEW bits and would not need to saturate. This operation is partly covered by the `vmulhu` and `vmulhsu` instructions, for the case where rounding is simply truncation (`rdn`).

13.4. Vector Single-Width Scaling Shift Instructions

These instructions shift the input value right, and round off the shifted out bits according to `vxrm`. The scaling right shifts have both zero-extending (vsrs1) and sign-extending (vssr1a) forms. The low \(\log_2(\text{SEW})\) bits of the vector or scalar shift-amount value are used; shift-amount immediates are zero-extended.

# Scaling shift right logical
vssrl.vv vd, vs2, vs1, vm  # vd[i] = roundoff_unsigned(vs2[i], vs1[i])
vssrl.vx vd, vs2, Rs1, vm  # vd[i] = roundoff_unsigned(vs2[i], x[rs1])
vssrl.vi vd, vs2, uimm, vm  # vd[i] = roundoff_unsigned(vs2[i], uimm)

# Scaling shift right arithmetic
vssra.vv vd, vs2, vs1, vm  # vd[i] = roundoff_signed(vs2[i], vs1[i])
vssra.vx vd, vs2, Rs1, vm  # vd[i] = roundoff_signed(vs2[i], x[rs1])
vssra.vi vd, vs2, uimm, vm  # vd[i] = roundoff_signed(vs2[i], uimm)

13.5. Vector Narrowing Fixed-Point Clip Instructions

The `vnclip` instructions are used to pack a fixed-point value into a narrower destination. The instructions support rounding, scaling, and saturation into the final destination format.
The second argument (vector element, scalar value, immediate value) gives the amount to right shift the source as in the narrowing shift instructions, which provides the scaling. The low \( \log_2(2 \times \text{SEW}) \) bits of the vector or scalar shift-amount value are used (e.g., the low 6 bits for a SEW=64-bit to SEW=32-bit narrowing operation). The immediate forms zero-extend their shift-amount immediate operand.

### Narrowing unsigned clip

<table>
<thead>
<tr>
<th>Instruction</th>
<th>SEW</th>
<th>2*SEW</th>
<th>SEW</th>
</tr>
</thead>
<tbody>
<tr>
<td>vnclipu.wv vd, vs2, vs1, vm</td>
<td># vd[i] = clip(roundoff_unsigned(vs2[i], vs1[i]))</td>
<td></td>
<td></td>
</tr>
<tr>
<td>vnclipu.wx vd, vs2, rs1, vm</td>
<td># vd[i] = clip(roundoff_unsigned(vs2[i], x[rs1]))</td>
<td></td>
<td></td>
</tr>
<tr>
<td>vnclipu.wi vd, vs2, uimm, vm</td>
<td># vd[i] = clip(roundoff_unsigned(vs2[i], uimm5))</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Narrowing signed clip

<table>
<thead>
<tr>
<th>Instruction</th>
<th>SEW</th>
<th>2*SEW</th>
<th>SEW</th>
</tr>
</thead>
<tbody>
<tr>
<td>vnclip.wv vd, vs2, vs1, vm</td>
<td># vd[i] = clip(roundoff_signed(vs2[i], vs1[i]))</td>
<td></td>
<td></td>
</tr>
<tr>
<td>vnclip.wx vd, vs2, rs1, vm</td>
<td># vd[i] = clip(roundoff_signed(vs2[i], x[rs1]))</td>
<td></td>
<td></td>
</tr>
<tr>
<td>vnclip.wi vd, vs2, uimm, vm</td>
<td># vd[i] = clip(roundoff_signed(vs2[i], uimm5))</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

For `vnclipu`/`vnclip`, the rounding mode is specified in the vxrm CSR. Rounding occurs around the least-significant bit of the destination and before saturation.

For `vnclipu`, the shifted rounded source value is treated as an unsigned integer and saturates if the result would overflow the destination viewed as an unsigned integer.

**Note**
There is no single instruction that can saturate a signed value into an unsigned destination. A sequence of two vector instructions that first removes negative numbers by performing a max against 0 using `vmax`, then clips the resulting unsigned value into the destination using `vnclipu`, can be used if setting `vxsat` value is not required. A `vsetvlq` is required inbetween these two instructions to change SEW.

For `vnclip`, the shifted rounded source value is treated as a signed integer and saturates if the result would overflow the destination viewed as a signed integer.

If any destination element is saturated, the `vxsat` bit is set in the `vxsat` register.
14. Vector Floating-Point Instructions

The standard vector floating-point instructions treat 16-bit, 32-bit, 64-bit, and 128-bit elements as IEEE-754/2008-compatible values. If the EEW of a vector floating-point operand does not correspond to a supported IEEE floating-point type, the instruction encoding is reserved.

**Note** The floating-point element widths that are supported depend on the profile.

Vector floating-point instructions require the presence of base scalar floating-point extensions corresponding to the supported vector floating-point element widths.

**Note** In particular, vector profiles supporting 16-bit half-precision floating-point values will also have to implement scalar half-precision floating-point support in the `f` registers.

If the floating-point unit status field `mstatus.FS` is *Off* then any attempt to execute a vector floating-point instruction will raise an illegal instruction exception. Any vector floating-point instruction that modifies any floating-point extension state (i.e., floating-point CSRs or `f` registers) must set `mstatus.FS` to *Dirty*.

The vector floating-point instructions have the same behavior as the scalar floating-point instructions with regard to NaNs.

Scalar values for vector-scalar operations can be sourced from the standard scalar `f` registers, as described in Section Vector Arithmetic Instruction encoding.

14.1. Vector Floating-Point Exception Flags

A vector floating-point exception at any active floating-point element sets the standard FP exception flags in the `fflags` register. Inactive elements do not set FP exception flags.

14.2. Vector Single-Width Floating-Point Add/Subtract Instructions

```plaintext
# Floating-point add
vfadd.vv vd, vs2, vs1, vm   # Vector-vector
vfadd.vf vd, vs2, rs1, vm   # vector-scalar

# Floating-point subtract
vfsub.vv vd, vs2, vs1, vm   # Vector-vector
vfsub.vf vd, vs2, rs1, vm   # Vector-scalar vd[i] = vs2[i] - f[rs1]
vfsub.vf vd, vs2, rs1, vm   # Scalar-vector vd[i] = f[rs1] - vs2[i]
```

14.3. Vector Widening Floating-Point Add/Subtract Instructions

```plaintext
# Widening FP add/subtract, 2*SEW = SEW +/- SEW
vfwadd.vv vd, vs2, vs1, vm   # vector-vector
vfwadd.vf vd, vs2, rs1, vm   # vector-scalar
vfwsub.vv vd, vs2, vs1, vm   # vector-vector
vfwsub.vf vd, vs2, rs1, vm   # vector-scalar

# Widening FP add/subtract, 2*SEW = 2*SEW +/- SEW
vfwadd.wv vd, vs2, vs1, vm   # vector-vector
vfwadd.wf vd, vs2, rs1, vm   # vector-scalar
vfwsub.wv vd, vs2, vs1, vm   # vector-vector
vfwsub.wf vd, vs2, rs1, vm   # vector-scalar
```

14.4. Vector Single-Width Floating-Point Multiply/Divide Instructions
# Floating-point multiply

\[
\text{vfmul.vv } vd, vs2, vs1, vm \quad \# \text{Vector-vector}
\]

\[
\text{vfmul.vf } vd, vs2, rs1, vm \quad \# \text{vector-scalar}
\]

# Floating-point divide

\[
\text{vfdiv.vv } vd, vs2, vs1, vm \quad \# \text{Vector-vector}
\]

\[
\text{vfdiv.vf } vd, vs2, rs1, vm \quad \# \text{vector-scalar}
\]

# Reverse floating-point divide vector = scalar / vector

\[
\text{vfrdiv.vf } vd, vs2, rs1, vm \quad \# \text{scalar-vector, } vd[i] = f[rs1]/vs2[i]
\]

## 14.5. Vector Widening Floating-Point Multiply

# Widening floating-point multiply

\[
\text{vfwmul.vv } vd, vs2, vs1, vm \quad \# \text{vector-vector}
\]

\[
\text{vfwmul.vf } vd, vs2, rs1, vm \quad \# \text{vector-scalar}
\]

## 14.6. Vector Single-Width Floating-Point Fused Multiply-Add Instructions

All four varieties of fused multiply-add are provided, and in two destructive forms that overwrite one of the operands, either the addend or the first multiplicand.

# FP multiply-accumulate, overwrites addend

\[
\text{vfmac.ccv } vd, vs1, vs2, vm \quad \# vd[i] = +(vs1[i] * vs2[i]) + vd[i]
\]

\[
\text{vfmac.vf } vd, rs1, vs2, vm \quad \# vd[i] = +(f[rs1] * vs2[i]) + vd[i]
\]

# FP negate-(multiply-accumulate), overwrites subtrahend

\[
\text{vfnmacc.ccv } vd, vs1, vs2, vm \quad \# vd[i] = -(vs1[i] * vs2[i]) - vd[i]
\]

\[
\text{vfnmacc.vf } vd, rs1, vs2, vm \quad \# vd[i] = -(f[rs1] * vs2[i]) - vd[i]
\]

# FP multiply-subtract-accumulator, overwrites subtrahend

\[
\text{vfmsac.ccv } vd, vs1, vs2, vm \quad \# vd[i] = +(vs1[i] * vs2[i]) - vd[i]
\]

\[
\text{vfmsac.vf } vd, rs1, vs2, vm \quad \# vd[i] = +(f[rs1] * vs2[i]) - vd[i]
\]

# FP negate-(multiply-subtract-accumulator), overwrites minuend

\[
\text{vfnmmsac.ccv } vd, vs1, vs2, vm \quad \# vd[i] = -(vs1[i] * vs2[i]) + vd[i]
\]

\[
\text{vfnmmsac.vf } vd, rs1, vs2, vm \quad \# vd[i] = -(f[rs1] * vs2[i]) + vd[i]
\]

# FP multiply-add, overwrites multiplicand

\[
\text{vfmad.ccv } vd, vs1, vs2, vm \quad \# vd[i] = +(vs1[i] * vd[i]) + vs2[i]
\]

\[
\text{vfmad.vf } vd, rs1, vs2, vm \quad \# vd[i] = +(f[rs1] * vd[i]) + vs2[i]
\]

# FP negate-(multiply-add), overwrites multiplicand

\[
\text{vfnmadd.ccv } vd, vs1, vs2, vm \quad \# vd[i] = -(vs1[i] * vd[i]) - vs2[i]
\]

\[
\text{vfnmadd.vf } vd, rs1, vs2, vm \quad \# vd[i] = -(f[rs1] * vd[i]) - vs2[i]
\]

# FP multiply-sub, overwrites multiplicand

\[
\text{vfmsub.ccv } vd, vs1, vs2, vm \quad \# vd[i] = +(vs1[i] * vd[i]) - vs2[i]
\]

\[
\text{vfmsub.vf } vd, rs1, vs2, vm \quad \# vd[i] = +(f[rs1] * vd[i]) - vs2[i]
\]

# FP negate-(multiply-sub), overwrites multiplicand

\[
\text{vfnmsub.ccv } vd, vs1, vs2, vm \quad \# vd[i] = -(vs1[i] * vd[i]) + vs2[i]
\]

\[
\text{vfnmsub.vf } vd, rs1, vs2, vm \quad \# vd[i] = -(f[rs1] * vd[i]) + vs2[i]
\]

*Note* It would be possible to use the two unused rounding modes in the scalar FP FMA encoding to provide a few non-destructive FMAs. However, this would be the only maskable operation with three inputs and separate output.

## 14.7. Vector Widening Floating-Point Fused Multiply-Add Instructions
The widening floating-point fused multiply-add instructions all overwrite the wide addend with the result. The multiplier inputs are all SEW wide, while the addend and destination is 2*SEW bits wide.

# FP widening multiply-accumulate, overwrites addend
vfwmacc.vv vd, vs1, vs2, vm  # vd[i] = +(vs1[i] * vs2[i]) + vd[i]
vfwmacc.vf vd, rs1, vs2, vm  # vd[i] = +(f[rs1] * vs2[i]) + vd[i]

# FP widening negate-(multiply-accumulate), overwrites addend
vfwmacc.vv vd, vs1, vs2, vm  # vd[i] = -(vs1[i] * vs2[i]) - vd[i]
vfwmacc.vf vd, rs1, vs2, vm  # vd[i] = -(f[rs1] * vs2[i]) - vd[i]

# FP widening multiply-subtract-accumulator, overwrites addend
vfwmsac.vv vd, vs1, vs2, vm  # vd[i] = +(vs1[i] * vs2[i]) - vd[i]
vfwmsac.vf vd, rs1, vs2, vm  # vd[i] = +(f[rs1] * vs2[i]) - vd[i]

# FP widening negate-(multiply-subtract-accumulator), overwrites addend
vfwmsac.vv vd, vs1, vs2, vm  # vd[i] = -(vs1[i] * vs2[i]) + vd[i]
vfwmsac.vf vd, rs1, vs2, vm  # vd[i] = -(f[rs1] * vs2[i]) + vd[i]

### 14.8. Vector Floating-Point Square-Root Instruction

This is a unary vector-vector instruction.

# Floating-point square root
vfsqrt.v vd, vs2, vm  # Vector-vector square root

### 14.9. Vector Floating-Point Reciprocal Square-Root Estimate Instruction

# Floating-point reciprocal square-root estimate to 7 bits.
vfrsqrtp7.v vd, vs2, vm

This is a unary vector-vector instruction that returns an estimate of 1/sqrt(x) accurate to 7 bits.

Note: An earlier draft version had used the assembler name vfrsqrtp7 but this was deemed to cause confusion with the ex notation for element width. The earlier name can be retained as alias in tool chains for backward compatibility.

The following table describes the instruction’s behavior for all classes of floating-point inputs:

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
<th>Exceptions raised</th>
</tr>
</thead>
<tbody>
<tr>
<td>-∞ ≤ x &lt; -0.0</td>
<td>canonical NaN</td>
<td>NV</td>
</tr>
<tr>
<td>-0.0</td>
<td>-∞</td>
<td>DZ</td>
</tr>
<tr>
<td>+0.0</td>
<td>+∞</td>
<td>DZ</td>
</tr>
<tr>
<td>+0.0 &lt; x &lt; +∞</td>
<td>estimate of 1/sqrt(x)</td>
<td></td>
</tr>
<tr>
<td>+∞</td>
<td>+0.0</td>
<td></td>
</tr>
<tr>
<td>qNaN</td>
<td>canonical NaN</td>
<td></td>
</tr>
<tr>
<td>sNaN</td>
<td>canonical NaN</td>
<td></td>
</tr>
</tbody>
</table>

Note: All positive normal and subnormal inputs produce normal outputs.

Note: The output value is independent of the dynamic rounding mode.

For the non-exceptional cases, the low bit of the exponent and the six high bits of significand (after the leading one) are concatenated and used to address the following table. The output of the table becomes the seven high bits of the result significand (after the leading one); the remainder of the result significand is zero. Subnormal inputs are normalized and the exponent adjusted appropriately before the lookup. The output exponent is chosen to make the result approximate the reciprocal of the square root of the argument.
More precisely, the result is computed as follows. Let the normalized input exponent be equal to the input exponent if the input is normal, or 0 minus the number of leading zeros in the significand otherwise. If the input is subnormal, the normalized input significand is given by shifting the input significand left by 1 minus the normalized input exponent, discarding the leading 1 bit. The output exponent equals floor((3*B - 1 - the normalized input exponent) / 2). The output sign equals the input sign.

The following table gives the seven MSBs of the output significand as a function of the LSB of the normalized input exponent and the six MSBs of the normalized input significand; the other bits of the output significand are zero.
<table>
<thead>
<tr>
<th>exp[0]</th>
<th>sig[MSB -: 6]</th>
<th>sig_out[MSB -: 7]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>52</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>51</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>50</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>48</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>47</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>46</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>44</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>43</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>42</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td>41</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>40</td>
</tr>
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29  84
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51  63
52  62
53  61
54  60
55  59
56  59
57  58
58  57
59  56
60  56
61  55
62  54
63  53

Note
For example, when SEW=32, vfrsqrt7(0x00718abc (∼= 1.043e-38)) = 0x5f080000 (∼= 9.800e18), and vfrsqrt7(0x7f765432 (∼= 3.274e38)) = 0x1f820000 (∼= 5.506e-20).

Note
The 7 bit accuracy was chosen as it requires 0,1,2,3 Newton-Raphson iterations to converge to close to bfloat16, FP16, FP32, FP64 accuracy respectively. Future instructions can be defined with greater estimate accuracy.

14.10. Vector Floating-Point Reciprocal Estimate Instruction

# Floating-point reciprocal estimate to 7 bits.
vrec7.v vd, vs2, vm

Note
An earlier draft version had used the assembler name vfrece7 but this was deemed to cause confusion with ex notation for element width. The earlier name can be retained as alias in tool chains for backward compatibility.

This is a unary vector-vector instruction that returns an estimate of 1/x accurate to 7 bits.
The following table describes the instruction's behavior for all classes of floating-point inputs, where $B$ is the exponent bias:

<table>
<thead>
<tr>
<th>Input ($x$)</th>
<th>Rounding Mode</th>
<th>Output ($y \approx 1/x$)</th>
<th>Exceptions raised</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-\infty$</td>
<td>any</td>
<td>-0.0</td>
<td></td>
</tr>
<tr>
<td>$-2^{B+1} &lt; x \leq -2^B$ (normal)</td>
<td>any</td>
<td>$-2^{-(B+1)} \geq y &gt; -2^B$ (subnormal, sig=01...)</td>
<td></td>
</tr>
<tr>
<td>$-2^B &lt; x \leq -2^{B+1}$ (normal)</td>
<td>any</td>
<td>$-2^B \geq y &gt; -2^{B+1}$ (subnormal, sig=1...)</td>
<td></td>
</tr>
<tr>
<td>$-2^{B-1} &lt; x \leq -2^{B+1}$ (normal)</td>
<td>any</td>
<td>$-2^{B+1} \geq y &gt; -2^B$ (normal)</td>
<td></td>
</tr>
<tr>
<td>$-2^{B+1} &lt; x \leq -2^B$ (subnormal, sig=1...)</td>
<td>any</td>
<td>$-2^{B+1} \geq y &gt; -2^B$ (normal)</td>
<td></td>
</tr>
<tr>
<td>$-2^B &lt; x \leq -2^{B+1}$ (subnormal, sig=01...)</td>
<td>any</td>
<td>$-2^B \geq y &gt; -2^{B+1}$ (normal)</td>
<td></td>
</tr>
<tr>
<td>$-2^{-(B+1)} &lt; x &lt; -0.0$ (subnormal, sig=00...)</td>
<td>RUP, RTZ</td>
<td>greatest-mag. negative finite value</td>
<td>NX, OF</td>
</tr>
<tr>
<td>$-2^{-(B+1)} &lt; x &lt; -0.0$ (subnormal, sig=00...)</td>
<td>RDN, RNE, RMM</td>
<td>-∞</td>
<td>NX, OF</td>
</tr>
<tr>
<td>$-0.0$</td>
<td>any</td>
<td>-∞</td>
<td>DZ</td>
</tr>
<tr>
<td>+0.0</td>
<td>any</td>
<td>+∞</td>
<td>DZ</td>
</tr>
<tr>
<td>$+0.0 &lt; x &lt; 2^{-(B+1)}$ (subnormal, sig=00...)</td>
<td>RUP, RNE, RMM</td>
<td>+∞</td>
<td>NX, OF</td>
</tr>
<tr>
<td>$0.0 &lt; x &lt; 2^{-(B+1)}$ (subnormal, sig=00...)</td>
<td>RDN, RTZ</td>
<td>greatest finite value</td>
<td>NX, OF</td>
</tr>
<tr>
<td>$2^{-(B+1)} \leq x &lt; 2^B$ (subnormal, sig=01...)</td>
<td>any</td>
<td>$2^{B+1} \geq y &gt; 2^B$ (normal)</td>
<td></td>
</tr>
<tr>
<td>$2^B \leq x &lt; 2^{B+1}$ (subnormal, sig=1...)</td>
<td>any</td>
<td>$2^B \geq y \geq 2^{B+1}$ (normal)</td>
<td></td>
</tr>
<tr>
<td>$2^{B+1} \leq x &lt; 2^{B+1}$ (normal)</td>
<td>any</td>
<td>$2^{B+1} \geq y \geq 2^{B+1}$ (normal)</td>
<td></td>
</tr>
<tr>
<td>$2^{B-1} \leq x &lt; 2^B$ (normal)</td>
<td>any</td>
<td>$2^{B+1} \geq y &gt; 2^B$ (subnormal, sig=1...)</td>
<td></td>
</tr>
<tr>
<td>$2^B \leq x &lt; 2^{B+1}$ (normal)</td>
<td>any</td>
<td>$2^B \geq y \geq 2^{-(B+1)}$ (subnormal, sig=01...)</td>
<td></td>
</tr>
<tr>
<td>$+\infty$</td>
<td>any</td>
<td>+0.0</td>
<td></td>
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<tr>
<td>NaN</td>
<td>any</td>
<td>canonical NaN</td>
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<tr>
<td>NaN</td>
<td>any</td>
<td>canonical NaN</td>
<td></td>
</tr>
</tbody>
</table>

**Note**

Subnormal inputs with magnitude at least $2^{-(B+1)}$ produce normal outputs; other subnormal inputs produce infinite outputs. Normal inputs with magnitude at least $2^{B-1}$ produce subnormal outputs; other normal inputs produce normal outputs.

The output value depends on the dynamic rounding mode when the overflow exception is raised.

For the non-exceptional cases, the seven high bits of significand (after the leading one) are used to address the following table. The output of the table becomes the seven high bits of the result significand (after the leading one); the remainder of the result significand is zero. Subnormal inputs are normalized and the exponent adjusted appropriately before the lookup. The output exponent is chosen to make the result approximate the reciprocal of the argument, and subnormal outputs are denormalized accordingly.

More precisely, the result is computed as follows. Let the normalized input exponent be equal to the input exponent if the input is normal, or 0 minus the number of leading zeros in the significand otherwise. The normalized output exponent equals $(2^B - 1 \cdot$ the normalized input exponent). If the normalized output exponent is outside the range $[-1, 2^B]$, the result corresponds to one of the exceptional cases in the table above.

If the input is subnormal, the normalized input significand is given by shifting the input significand left by 1 minus the normalized input exponent, discarding the leading 1 bit. Otherwise, the normalized input significand equals the input significand. The following table gives the seven MSBs of the normalized output significand as a function of the seven MSBs of the normalized input significand; the other bits of the normalized output significand are zero.
Table 18. vfrec7.v common-case lookup table contents

<table>
<thead>
<tr>
<th>sig[MSB -: 7]</th>
<th>sig_out[MSB -: 7]</th>
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<tbody>
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</table>
If the normalized output exponent is 0 or -1, the result is subnormal: the output exponent is 0, and the output significand is
given by concatenating a 1 bit to the left of the normalized output significand, then shifting that quantity right by 1 minus the
normalized output exponent. Otherwise, the output exponent equals the normalized output exponent, and the output
significand equals the normalized output significand. The output sign equals the input sign.

Note
For example, when SEW=32, vfrec7(0x00718abc (≈ 1.043e-38)) = 0x7e900000 (≈ 9.570e37), and vfrec7(0x7f765432 (≈ 3.274e38))
= 0x00214000 (≈ 3.053e-39).

Note
The 7 bit accuracy was chosen as it requires 0.1.2,3 Newton-Raphson iterations to converge to close to bfloat16, FP16, FP32, FP64
accuracy respectively. Future instructions can be defined with greater estimate accuracy.

14.11. Vector Floating-Point MIN/MAX Instructions

The vector floating-point vfmin and vfmax instructions have the same behavior as the corresponding scalar floating-point
instructions in version 2.2 of the RISC-V F/D/Q extension.
**14.12. Vector Floating-Point Sign-Injection Instructions**

Vector versions of the scalar sign-injection instructions. The result takes all bits except the sign bit from the vector \( vs2 \) operands.

```
# Floating-point minimum
vfmin.vv vd, vs2, vs1, vm  # Vector-vector
vfmin.vf vd, vs2, rs1, vm   # vector-scalar

# Floating-point maximum
vfmax.vv vd, vs2, vs1, vm   # Vector-vector
vfmax.vf vd, vs2, rs1, vm   # vector-scalar
```

**Note**
A vector of floating-point values can be negated using a sign-injection instruction with both source operands set to the same vector operand. Can define assembly pseudoinstruction `vfneg.v vd, vs = vfsgnjn.vv vd, vs, vs`.

**14.13. Vector Floating-Point Compare Instructions**

These vector FP compare instructions compare two source operands and write the comparison result to a mask register. The destination mask vector is always held in a single vector register, with a layout of elements as described in Section Mask Register Layout. The destination mask vector register may be the same as the source vector mask register (v0). Comparisons write mask registers, and so always operate under a tail-agnostic policy.

The compare instructions follow the semantics of the scalar floating-point compare instructions. `vmfeq` and `vmfne` raise the invalid operation exception only on signaling NaN inputs. `vmflt`, `vmfle`, `vmfgt`, and `vmfge` raise the invalid operation exception on both signaling and quiet NaN inputs. `vmfne` writes 1 to the destination element when either operand is NaN, whereas the other comparisons write 0 when either operand is NaN.

```
# Compare equal
vmfeq.vv vd, vs2, vs1, vm  # Vector-vector
vmfeq.vf vd, vs2, rs1, vm   # vector-scalar

# Compare not equal
vmfne.vv vd, vs2, vs1, vm   # Vector-vector
vmfne.vf vd, vs2, rs1, vm   # vector-scalar

# Compare less than
vmflt.vv vd, vs2, vs1, vm   # Vector-vector
vmflt.vf vd, vs2, rs1, vm   # vector-scalar

# Compare less than or equal
vmfle.vv vd, vs2, vs1, vm   # Vector-vector
vmfle.vf vd, vs2, rs1, vm   # vector-scalar

# Compare greater than
vmfgt.vf vd, vs2, rs1, vm   # vector-scalar

# Compare greater than or equal
vmfge.vf vd, vs2, rs1, vm   # vector-scalar
```
<table>
<thead>
<tr>
<th>Comparison</th>
<th>Assembler Mapping</th>
<th>Assembler pseudoinstruction</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>va &lt; vb</code></td>
<td><code>vmflt.vv vd, va, vb, vm</code></td>
<td></td>
</tr>
<tr>
<td><code>va &lt;= vb</code></td>
<td><code>vmfle.vv vd, va, vb, vm</code></td>
<td></td>
</tr>
<tr>
<td><code>va &gt; vb</code></td>
<td><code>vmflt.vv vd, vb, va, vm</code></td>
<td><code>vmfgt.vv vd, va, vb, vm</code></td>
</tr>
<tr>
<td><code>va &gt;= vb</code></td>
<td><code>vmfle.vv vd, vb, va, vm</code></td>
<td><code>vmfge.vv vd, va, vb, vm</code></td>
</tr>
<tr>
<td><code>va &lt; f</code></td>
<td><code>vmflt.vf vd, va, f, vm</code></td>
<td></td>
</tr>
<tr>
<td><code>va &lt;= f</code></td>
<td><code>vmfle.vf vd, va, f, vm</code></td>
<td></td>
</tr>
<tr>
<td><code>va &gt; f</code></td>
<td><code>vmfgt.vf vd, va, f, vm</code></td>
<td></td>
</tr>
<tr>
<td><code>va &gt;= f</code></td>
<td><code>vmfge.vf vd, va, f, vm</code></td>
<td></td>
</tr>
</tbody>
</table>

`va, vb` vector register groups  
`f` scalar floating-point register

**Note**
Providing all forms is necessary to correctly handle unordered comparisons for NaNs.

**Note**
C99 floating-point quiet comparisons can be implemented by masking the signaling comparisons when either input is NaN, as follows. When the comparand is a non-NaN constant, the middle two instructions can be omitted.

```c
# Example of implementing isgreater()
vmfle.vv v0, va, va        # Only set where A is not NaN.
vmfle.vv v1, vb, vb        # Only set where B is not NaN.
vmand.mm v0, v0, v1        # Only set where A and B are ordered,
vmfge.vv v0, va, vb, v0.t  # so only set flags on ordered values.
```

**Note**
In the above sequence, it is tempting to mask the second `vmfle` instruction and remove the `vmand` instruction, but this more efficient sequence incorrectly fails to raise the invalid exception when an element of `va` contains a quiet NaN and the corresponding element in `vb` contains a signaling NaN.

### 14.14. Vector Floating-Point Classify Instruction

This is a unary vector-vector instruction that operates in the same way as the scalar classify instruction.

```
vfclass.v vd, vs2, vm   # Vector-vector
```

The 10-bit mask produced by this instruction is placed in the least-significant bits of the result elements. The upper (SEW-10) bits of the result are filled with zeros. The instruction is only defined for SEW=16b and above, so the result will always fit in the destination elements.

### 14.15. Vector Floating-Point Merge Instruction

A vector-scalar floating-point merge instruction is provided, which operates on all body elements, from `vstart` up to the current vector length in `vl` regardless of mask value.

The `vfmerge.vfm` instruction is encoded as a masked instruction (vm=0). At elements where the mask value is zero, the first vector operand is copied to the destination element, otherwise a scalar floating-point register value is copied to the destination element.

```
vfmerge.vfm vd, vs2, rs1, v0  # vd[i] = v0.mask[i] ? f[rs1] : vs2[i]
```

### 14.16. Vector Floating-Point Move Instruction

The vector floating-point move instruction `splats` a floating-point scalar operand to a vector register group. The instruction copies a scalar `f` register value to all active elements of a vector register group. This instruction is encoded as a masked instruction (vm=1). The instruction must have the `vs2` field set to `v0`, with all other values for `vs2` reserved.

```
vfmv.v.f vd, rs1  # vd[i] = f[rs1]
```
Note: The vfmv.v.f instruction shares the encoding with the vfmerge.vfm instruction, but with vm=1 and vs2=v0.

14.17. Single-Width Floating-Point/Integer Type-Convert Instructions

Conversion operations are provided to convert to and from floating-point values and unsigned and signed integers, where both source and destination are SEW wide.

\[
\begin{align*}
&\text{vfcvt.xu.f.v vd, vs2, vm} & \text{# Convert float to unsigned integer.} \\
&\text{vfcvt.x.f.v vd, vs2, vm} & \text{# Convert float to signed integer.} \\
&\text{vfcvt.rtz.xu.f.v vd, vs2, vm} & \text{# Convert float to unsigned integer, truncating.} \\
&\text{vfcvt.rtz.x.f.v vd, vs2, vm} & \text{# Convert float to signed integer, truncating.} \\
&\text{vfcvt.f.xu.v vd, vs2, vm} & \text{# Convert unsigned integer to float.} \\
&\text{vfcvt.f.x.v vd, vs2, vm} & \text{# Convert signed integer to float.}
\end{align*}
\]

The conversions follow the same rules on exceptional conditions as the scalar conversion instructions. The conversions use the dynamic rounding mode in frm, except for the rtz variants, which round towards zero.

Note: The rtz variants are provided to accelerate truncating conversions from floating-point to integer, as is common in languages like C and Java.

14.18. Widening Floating-Point/Integer Type-Convert Instructions

A set of conversion instructions is provided to convert between narrower integer and floating-point datatypes to a type of twice the width.

\[
\begin{align*}
&\text{vfwcvt.xu.f.v vd, vs2, vm} & \text{# Convert float to double-width unsigned integer.} \\
&\text{vfwcvt.x.f.v vd, vs2, vm} & \text{# Convert float to double-width signed integer.} \\
&\text{vfwcvt.rtz.xu.f.v vd, vs2, vm} & \text{# Convert float to double-width unsigned integer, truncating.} \\
&\text{vfwcvt.rtz.x.f.v vd, vs2, vm} & \text{# Convert float to double-width signed integer, truncating.} \\
&\text{vfwcvt.f.xu.v vd, vs2, vm} & \text{# Convert unsigned integer to double-width float.} \\
&\text{vfwcvt.f.x.v vd, vs2, vm} & \text{# Convert signed integer to double-width float.} \\
&\text{vfwcvt.f.f.v vd, vs2, vm} & \text{# Convert single-width float to double-width float.}
\end{align*}
\]

These instructions have the same constraints on vector register overlap as other widening instructions (see Widening Vector Arithmetic Instructions).

Note: A double-width IEEE floating-point value can always represent a single-width integer exactly.

Note: A double-width IEEE floating-point value can always represent a single-width IEEE floating-point value exactly.

Note: A full set of floating-point widening conversions is not supported as single instructions, but any widening conversion can be implemented as several doubling steps with equivalent results and no additional exception flags raised.

14.19. Narrowing Floating-Point/Integer Type-Convert Instructions

A set of conversion instructions is provided to convert wider integer and floating-point datatypes to a type of half the width.
vfncvt.x.u.f.w vd, vs2, vm       # Convert double-width float to unsigned integer.
vfncvt.x.f.w vd, vs2, vm       # Convert double-width float to signed integer.

vfncvt.rtz.x.u.f.w vd, vs2, vm   # Convert double-width float to unsigned integer, truncating.
vfncvt.rtz.x.f.w vd, vs2, vm   # Convert double-width float to signed integer, truncating.

vfncvt.f.x.u.w vd, vs2, vm       # Convert double-width unsigned integer to float.
vfncvt.f.x.w vd, vs2, vm       # Convert double-width signed integer to float.

vfncvt.f.f.w vd, vs2, vm       # Convert double-width float to single-width float.
vfncvt.rod.f.f.w vd, vs2, vm    # Convert double-width float to single-width float, rounding towards odd.

These instructions have the same constraints on vector register overlap as other narrowing instructions (see Narrowing Vector Arithmetic Instructions).

Note: A full set of floating-point widening conversions is not supported as single instructions. Conversions can be implemented in a sequence of halving steps. Results are equivalently rounded and the same exception flags are raised if all but the last halving step use round-towards-odd (vfncvt.rod.f.f.w). Only the final step should use the desired rounding mode.
15. Vector Reduction Operations

Vector reduction operations take a vector register group of elements and a scalar held in element 0 of a vector register, and perform a reduction using some binary operator, to produce a scalar result in element 0 of a vector register. The scalar input and output operands are held in element 0 of a single vector register, not a vector register group, so any vector register can be the scalar source or destination of a vector reduction regardless of LMUL setting.

The destination vector register can overlap the source operands, including the mask register.

Note: Reductions read and write the scalar operand and result into element 0 of a vector register to avoid a loss of decoupling with the scalar processor, and to support future polymorphic use with future types not supported in the scalar unit.

Inactive elements from the source vector register group are excluded from the reduction, but the scalar operand is always included regardless of the mask values.

The other elements in the destination vector register (0 < index < VLEN/SEW) are considered the tail and are managed with the current tail agnostic/undisturbed policy.

If v1=0, no operation is performed and the destination register is not updated.

Traps on vector reduction instructions are always reported with a vstart of 0. Vector reduction operations raise an illegal instruction exception if vstart is non-zero.

The assembler syntax for a reduction operation is vredop vs, where the vs suffix denotes the first operand is a vector register group and the second operand is a scalar stored in element 0 of a vector register.

15.1. Vector Single-Width Integer Reduction Instructions

All operands and results of single-width reduction instructions have the same SEW width. Overflows wrap around on arithmetic sums.

# Simple reductions, where [*] denotes all active elements:
  vredsum vs vd, vs2, vs1, vm  # vd[0] = sum( vs1[0] , vs2[*] )
  vredmaxu vs vd, vs2, vs1, vm  # vd[0] = maxu( vs1[0] , vs2[*] )
  vredmax vs vd, vs2, vs1, vm  # vd[0] = max( vs1[0] , vs2[*] )
  vredminu vs vd, vs2, vs1, vm  # vd[0] = minu( vs1[0] , vs2[*] )
  vredmin vs vd, vs2, vs1, vm  # vd[0] = min( vs1[0] , vs2[*] )
  vredand vs vd, vs2, vs1, vm  # vd[0] = and( vs1[0] , vs2[*] )
  vredor vs vd, vs2, vs1, vm  # vd[0] = or( vs1[0] , vs2[*] )
  vredxor vs vd, vs2, vs1, vm  # vd[0] = xor( vs1[0] , vs2[*] )

15.2. Vector Widening Integer Reduction Instructions

The unsigned vwredsumu vs instruction zero-extends the SEW-wide vector elements before summing them, then adds the 2*SEW-width scalar element, and stores the result in a 2*SEW-width scalar element.

The vwredsum vs instruction sign-extends the SEW-wide vector elements before summing them.

# Unsigned sum reduction into double-width accumulator
  vwredsumu vs vd, vs2, vs1, vm  # 2*SEW = 2*SEW + sum(zero-extend(SEW))

# Signed sum reduction into double-width accumulator
  vwredsum vs vd, vs2, vs1, vm  # 2*SEW = 2*SEW + sum(sign-extend(SEW))

15.3. Vector Single-Width Floating-Point Reduction Instructions
# Simple reductions.

\[ \text{vfredosum} \text{.vs } v_d, v_{s2}, v_{s1}, v_m \ # \text{Ordered sum} \]

\[ \text{vfredsum} \text{.vs } v_d, v_{s2}, v_{s1}, v_m \ # \text{Unordered sum} \]

\[ \text{vfredmax} \text{.vs } v_d, v_{s2}, v_{s1}, v_m \ # \text{Maximum value} \]

\[ \text{vfredmin} \text{.vs } v_d, v_{s2}, v_{s1}, v_m \ # \text{Minimum value} \]

## 15.3.1. Vector Ordered Single-Width Floating-Point Sum Reduction

The \text{vfredosum} instruction must sum the floating-point values in element order, starting with the scalar in \( v_{s1}[0] \)--that is, it performs the computation:

\[ v_d[0] = (((v_{s1}[0] + v_{s2}[0]) + v_{s2}[1]) + \ldots) + v_{s2}[v_l-1] \]

where each addition operates identically to the scalar floating-point instructions in terms of raising exception flags and generating or propagating special values.

**Note** The ordered reduction supports compiler autovectorization, while the unordered FP sum allows for faster implementations.

When the operation is masked (\( v_m=0 \)), the masked-off elements do not affect the result or the exception flags.

**Note** If no elements are active, no additions are performed, so the scalar in \( v_{s1}[0] \) is simply copied to the destination register, without canonicalizing NaN values and without setting any exception flags. This behavior preserves the handling of NaNs, exceptions, and rounding when autovectorizing a scalar summation loop.

## 15.3.2. Vector Unordered Single-Width Floating-Point Sum Reduction

The unordered sum reduction instruction, \text{vfredsum}, provides an implementation more freedom in performing the reduction.

The implementation can produce a result equivalent to a reduction tree composed of binary operator nodes, with the inputs being elements from the source vector register group \( (v_{s2}) \) and the source scalar value \( (v_{s1}[0]) \). Each operator in the tree accepts two inputs and produces one result. Each operator first computes an exact sum as a RISC-V scalar floating-point addition with infinite exponent range and precision, then converts this exact sum to a floating-point format with range and precision each at least as great as the element floating-point format indicated by SEW, rounding using the currently active floating-point dynamic rounding mode. A different floating-point range and precision may be chosen for the result of each operator. A node where one input is derived only from elements masked-off or beyond the active vector length may either treat that input as the additive identity of the appropriate EEW or simply copy the other input to its output. The rounded result from the root node in the tree is converted (rounded again, using the dynamic rounding mode) to the standard floating-point format indicated by SEW. An implementation is allowed to add an additional additive identity to the final result.

The additive identity is +0.0 when rounding down (towards \(-\infty\)) or -0.0 for all other rounding modes.

The reduction tree structure must be deterministic for a given value in \( v_{\text{type}} \) and \( v_l \).

**Note** As a consequence of this definition, implementations need not propagate NaN payloads through the reduction tree when no elements are active. In particular, if no elements are active and the scalar input is NaN, implementations are permitted to canonicalize the NaN and, if the NaN is signaling, set the invalid exception flag. Implementations are alternatively permitted to pass through the original NaN and set no exception flags, as with \text{vfredosum}.

**Note** The \text{vfredosum} instruction is a valid implementation of the \text{vfredsum} instruction.

## 15.3.3. Vector Single-Width Floating-Point Max and Min Reductions

**Note** Floating-point max and min reductions should return the same final value and raise the same exception flags regardless of operation order.

**Note** If no elements are active, the scalar in \( v_{s1}[0] \) is simply copied to the destination register, without canonicalizing NaN values and without setting any exception flags.

## 15.4. Vector Widening Floating-Point Reduction Instructions
Widening forms of the sum reductions are provided that read and write a double-width reduction result.

```plaintext
# Simple reductions.
vfwredosum.vs vd, vs2, vs1, vm # Ordered sum
vfwredsum.vs vd, vs2, vs1, vm  # Unordered sum
```

The reduction of the SEW-width elements is performed as in the single-width reduction case, with the elements in `vs2` promoted to 2*SEW bits before adding to the 2*SEW-bit accumulator.

Note: `vfwredosum.vs` handles inactive elements and NaN payloads analogously to `vfredosum.vs`; `vfwredsum.vs` does so analogously to `vfredsum.vs`. 
16. Vector Mask Instructions

Several instructions are provided to help operate on mask values held in a vector register.

16.1. Vector Mask-Register Logical Instructions

Vector mask-register logical operations operate on mask registers. Each element in a mask register is a single bit, so these instructions all operate on single vector registers regardless of the setting of the v1mul field in vtype. They do not change the value of v1mul. The destination vector register may be the same as either source vector register.

As with other vector instructions, the elements with indices less than vstart are unchanged, and vstart is reset to zero after execution. Vector mask logical instructions are always unmasked so there are no inactive elements. Mask elements past v1, the tail elements, are always updated with a tail-agnostic policy.

```
vmand.mm vd, vs2, vs1     # vd.mask[i] =   vs2.mask[i] &&  vs1.mask[i]
vmandnot.mm vd, vs2, vs1  # vd.mask[i] = !(vs2.mask[i] &&  vs1.mask[i])
vmxor.mm vd, vs2, vs1     # vd.mask[i] =   vs2.mask[i] ^^  vs1.mask[i]
vnor.mm  vd, vs2, vs1     # vd.mask[i] =   vs2.mask[i] ||  vs1.mask[i]
vnornot.mm vd, vs2, vs1   # vd.mask[i] =   vs2.mask[i] || !vs1.mask[i]
vmxnor.mm vd, vs2, vs1    # vd.mask[i] = !(vs2.mask[i] ^^  vs1.mask[i])
```

Several assembler pseudoinstructions are defined as shorthand for common uses of mask logical operations:

```
vmmv.m vd, vs  => vmand.mm vd, vs, vs  # Copy mask register
vmclr.m vd     => vmxor.mm vd, vd, vd   # Clear mask register
vmset.m vd     => vmxnor.mm vd, vd, vd  # Set mask register
vmnot.m vd, vs => vmmv.m mm vd, vs      # Invert bits
```

Note: The vmmv.m instruction was previously called vmcpy.m, but with new layout it is more consistent to name as a "mv" because bits are copied without interpretation. The vmcpy.m assembler pseudo-instruction can be retained for compatibility.

The set of eight mask logical instructions can generate any of the 16 possibly binary logical functions of the two input masks:

<table>
<thead>
<tr>
<th>inputs</th>
<th>src1</th>
<th>src2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
### 16.2. Vector mask population count `vpopc`

* `vpopc.m rd, vs2, vm`

The source operand is a single vector register holding mask register values as described in Section [Mask Register Layout](#). The `vpopc.m` instruction counts the number of mask elements of the active elements of the vector source mask register that have the value 1 and writes the result to a scalar `x` register.

The operation can be performed under a mask, in which case only the masked elements are counted.

\[
\text{vpopc.m rd, vs2, v0.t} \# x[rd] = \sum_i (\text{vs2.mask}[i] \&\& \text{v0.mask}[i])
\]

Traps on `vpopc.m` are always reported with a `vstart` of 0. The `vpopc` instruction will raise an illegal instruction exception if `vstart` is non-zero.

### 16.3. `vfirst` find-first-set mask bit

* `vfirst.m rd, vs2, vm`

The `vfirst` instruction finds the lowest-numbered active element of the source mask vector that has the value 1 and writes that element’s index to a GPR. If no active element has the value 1, -1 is written to the GPR.

**Note** Software can assume that any negative value (highest bit set) corresponds to no element found, as vector lengths will never exceed \(2^{(XLEN-1)}\) on any implementation.

Traps on `vfirst` are always reported with a `vstart` of 0. The `vfirst` instruction will raise an illegal instruction exception if `vstart` is non-zero.

### 16.4. `vmsbf.m` set-before-first mask bit
vmsbf.m vd, vs2, vm

# Example

<table>
<thead>
<tr>
<th>Element number</th>
<th>v3 contents</th>
<th>v2 contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 6 5 4 3 2 1 0</td>
<td>1 0 0 1 0 1 0</td>
<td>0 0 0 0 0 0 1 1</td>
</tr>
<tr>
<td>1 0 0 1 0 1 0 1</td>
<td>0 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1 0 1 0 1 1 1 1</td>
<td>1 1 1 1 1 1 1 0</td>
<td>0 0 0 0 0 0 1 1</td>
</tr>
<tr>
<td>1 1 1 1 0 0 1 1</td>
<td>1 0 0 1 0 1 0 0</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1 0 0 0 0 0 0 0</td>
<td>1 1 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1 0 0 0 0 0 0 1</td>
<td>1 0 0 1 0 1 0 1</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>0 1 x x x x 1 1</td>
<td>0 0 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
</tbody>
</table>

The vmsbf.m instruction takes a mask register as input and writes results to a mask register. The instruction writes a 1 to all active mask elements before the first source element that is a 1, then writes a 0 to that element and all following active elements. If there is no set bit in the source vector, then all active elements in the destination are written with a 1.

The tail elements in the destination mask register are updated under a tail-agnostic policy.

Traps on vmsbf.m are always reported with a vstart of 0. The vmsbf instruction will raise an illegal instruction exception if vstart is non-zero.

The destination register cannot overlap the source register and, if masked, cannot overlap the mask register (v0).

16.5. vmsif.m set-including-first mask bit

The vector mask set-including-first instruction is similar to set-before-first, except it also includes the element with a set bit.

vmsif.m vd, vs2, vm

# Example

<table>
<thead>
<tr>
<th>Element number</th>
<th>v3 contents</th>
<th>v2 contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 6 5 4 3 2 1 0</td>
<td>1 0 0 1 0 1 0</td>
<td>0 0 0 0 0 0 1 1</td>
</tr>
<tr>
<td>1 0 0 1 0 1 0 1</td>
<td>0 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1 0 1 0 1 1 1 1</td>
<td>1 1 1 1 1 1 1 0</td>
<td>0 0 0 0 0 0 0 1</td>
</tr>
<tr>
<td>1 1 0 0 0 0 1 1</td>
<td>1 0 0 1 0 1 0 0</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1 0 0 0 0 0 0 0</td>
<td>1 1 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>0 0 0 0 0 0 0 0</td>
<td>1 0 0 1 0 1 0 0</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1 1 x x x x 1 1</td>
<td>0 0 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
</tbody>
</table>

The tail elements in the destination mask register are updated under a tail-agnostic policy.

Traps on vmsif.m are always reported with a vstart of 0. The vmsif instruction will raise an illegal instruction exception if vstart is non-zero.
The destination register cannot overlap the source register and, if masked, cannot overlap the mask register (‘v0’).

16.6. \texttt{vmsof.m} set-only-first mask bit

The vector mask set-only-first instruction is similar to set-before-first, except it only sets the first element with a bit set, if any.

\begin{verbatim}
vmsof.m vd, vs2, vm

# Example

7 6 5 4 3 2 1 0 Element number
1 0 0 1 0 1 0 0 v3 contents
vmsof.m v2, v3
0 0 0 0 1 0 0 v2 contents
1 0 0 1 0 1 0 1 v3 contents
vmsof.m v2, v3
0 0 0 0 0 0 1 v2

1 1 0 0 0 1 1 v0 vcontents
1 1 0 1 0 1 0 0 v3 contents
vmsof.m v2, v3, v0.t
0 1 x x x x 0 0 v2 contents
\end{verbatim}

The tail elements in the destination mask register are updated under a tail-agnostic policy.

Traps on \texttt{vmsof.m} are always reported with a \texttt{vstart} of 0. The \texttt{vmsof} instruction will raise an illegal instruction exception if \texttt{vstart} is non-zero.

The destination register cannot overlap the source register and, if masked, cannot overlap the mask register (‘v0’).

16.7. Example using vector mask instructions

The following is an example of vectorizing a data-dependent exit loop.

\begin{verbatim}
# char* strcpy(char *dst, const char* src)
strcpy:
    mv a2, a0             # Copy dst
    li t0, -1             # Infinite AVL
loop:
    vsetvli x0, t0, e8, m8, ta,ma # Max length vectors of bytes
    vle8ff.v v8, (a1)     # Get src bytes
    csrr t1, v1           # Get number of bytes fetched
    vmseq.vi v1, v8, 0    # Flag zero bytes
    vfirst.m a3, v1       # Zero found?
    add a1, a1, t1        # Bump pointer
    vmsif.m v0, v1        # Set mask up to and including zero byte.
    vse8.v v8, (a2), v0.t # Write out bytes
    add a2, a2, t1        # Bump pointer
    bltz a3, loop         # Zero byte not found, so loop
ret
\end{verbatim}
# char* strncpy(char *dst, const char* src, size_t n)

strncpy:
    mv a3, a0        # Copy dst

loop:
    vsetvli x0, a2, e8,m8, ta,ma   # Vectors of bytes.
    vle8ff.v v8, (a1)       # Get src bytes
    vmseq.vi v1, v8, 0     # Flag zero bytes
    csrr t1, v1            # Get number of bytes fetched
    vfirst.m a4, v1        # Zero found?
    vmsif.m v8, v1         # Set mask up to and including zero byte.
    vse8.v v8, (a3), v0.t  # Write out bytes
    sub a2, a2, t1         # Decrement count.
    bgez a4, zero_tail     # Zero remaining bytes.
    add a1, a1, t1         # Bump pointer
    add a3, a3, t1         # Bump pointer
    bnez a2, loop          # Anymore?

ret

zero_tail:
    vsetvli x0, a2, e8,m8, ta,ma   # Vectors of bytes.
    vmv.v.i v0, 0             # Splat zero.

zero_loop:
    vsetvli t1, a2, e8,m8, ta,ma  # Vectors of bytes.
    vse8.v v0, (a3)           # Store zero.
    sub a2, a2, t1           # Decrement count.
    add a3, a3, t1           # Bump pointer
    bnez a2, zero_loop       # Anymore?

ret

### 16.8. Vector Iota Instruction

The viota.m instruction reads a source vector mask register and writes to each element of the destination vector register group the sum of all the bits of elements in the mask register whose index is less than the element, e.g., a parallel prefix sum of the mask values.

This instruction can be masked, in which case only the enabled elements contribute to the sum and only the enabled elements are written.

viota.m vd, vs2, vm

# Example

```
    7 6 5 4 3 2 1 0   Element number
    1 0 0 1 0 0 1    v2 contents
    2 2 2 1 1 1 0    v4 result
    1 1 1 0 1 0 1    v0 contents
    1 0 0 1 0 0 1    v2 contents
    2 3 4 5 6 7 8 9  v4 contents
    1 1 1 5 1 7 1 0   v4 results
```

The result value is zero-extended to fill the destination element if SEW is wider than the result. If the result value would overflow the destination SEW, the least-significant SEW bits are retained.
Traps on `viota.m` are always reported with a `vstart` of 0, and execution is always restarted from the beginning when resuming after a trap handler. An illegal instruction exception is raised if `vstart` is non-zero.

The destination register group cannot overlap the source register and, if masked, cannot overlap the mask register (v0).

Note: These constraints exist for two reasons. First, to simplify avoidance of WAR hazards in implementations with temporally long vector registers and no vector register renaming. Second, to enable resuming execution after a trap simpler.

The `viota.m` instruction can be combined with memory scatter instructions (indexed stores) to perform vector compress functions.

```c
#include <stdio.h>

int main()
{
    int a0 = n;
    int a1 = &in;
    int a2 = &out;

    compact_non_zero:
    li a6, 0                      # Clear count of non-zero elements
    loop:
    vsetvli a5, a0, e32,m8,ta,ma   # 32-bit integers
    vle32.v v8, (a1)               # Load input vector
    add a0, a0, a5                 # Decrement number done
    slli a5, a5, 2                 # Multiply by four bytes
    vmsne.vi v0, v8, 0             # Locate non-zero values
    add a1, a1, a5                 # Bump input pointer
    viota.m v16, v0                # Get destination offsets of active elements
    add a6, a6, a5                 # Accumulate number of elements
    vsll.vi v16, v16, 2, v0.t      # Multiply offsets by four bytes
    slli a5, a5, 2                 # Multiply number of non-zero elements by four bytes
    vsuxel32.v v8, (a2), v16, v0.t # Scatter using scaled viota results under mask
    add a2, a2, a5                 # Bump output pointer
    bnez a0, loop                  # Any more?
    mv a0, a6                      # Return count
    ret
}
```

### 16.9. Vector Element Index Instruction

The `vid.v` instruction writes each element’s index to the destination vector register group, from 0 to `vl-1`.

```
vid.v vd, vm # Write element ID to destination.
```

The instruction can be masked.
The vs2 field of the instruction must be set to v0, otherwise the encoding is reserved.

The result value is zero-extended to fill the destination element if SEW is wider than the result. If the result value would overflow the destination SEW, the least-significant SEW bits are retained.

Note Microarchitectures can implement vid. v instruction using the same datapath as viota. m but with an implicit set mask source.
17. Vector Permutation Instructions

A range of permutation instructions are provided to move elements around within the vector registers.

17.1. Integer Scalar Move Instructions

The integer scalar read/write instructions transfer a single value between a scalar \( x \) register and element 0 of a vector register. The instructions ignore LMUL and vector register groups.

\[
\text{vmv.x.s } \text{rd, vs2} \quad \# \ x[\text{rd}] = \text{vs2}[0] \quad (\text{rs1}=0) \\
\text{vmv.s.x } \text{vd, rs1} \quad \# \ \text{vd}[0] = x[\text{rs1}] \quad (\text{vs2}=0)
\]

The \text{vmv.x.s} instruction copies a single SEW-wide element from index 0 of the source vector register to a destination integer register. If SEW > XLEN, the least-significant XLEN bits are transferred and the upper SEW-XLEN bits are ignored. If SEW < XLEN, the value is sign-extended to XLEN bits.

The \text{vmv.s.x} instruction copies the scalar integer register to element 0 of the destination vector register. If SEW < XLEN, the least-significant bits are copied and the upper XLEN-SEW bits are ignored. If SEW > XLEN, the value is sign-extended to SEW bits. The other elements in the destination vector register ( 0 < index < VLEN/SEW) are treated as tail elements using the current tail agnostic/undisturbed policy. If \( \text{vstart} \geq \text{vl} \), no operation is performed and the destination register is not updated.

Note: As a consequence, when \( \text{vl}=0 \), no elements are updated in the destination vector register group, regardless of \( \text{vstart} \).

The encodings corresponding to the masked versions (\( \text{vm}=0 \)) of \text{vmv.x.s} and \text{vmv.s.x} are reserved.

17.2. Floating-Point Scalar Move Instructions

The floating-point scalar read/write instructions transfer a single value between a scalar \( f \) register and element 0 of a vector register. The instructions ignore LMUL and vector register groups.

\[
\text{vfmv.f.s } \text{rd, vs2} \quad \# \ f[\text{rd}] = \text{vs2}[0] \quad (\text{rs1}=0) \\
\text{vfmv.s.f } \text{vd, rs1} \quad \# \ \text{vd}[0] = f[\text{rs1}] \quad (\text{vs2}=0)
\]

The \text{vfmv.f.s} instruction copies a single SEW-wide element from index 0 of the source vector register to a destination scalar floating-point register.

The \text{vfmv.s.f} instruction copies the scalar floating-point register to element 0 of the destination vector register. The other elements in the destination vector register ( 0 < index < VLEN/SEW) are treated as tail elements using the current tail agnostic/undisturbed policy. If \( \text{vstart} \geq \text{vl} \), no operation is performed and the destination register is not updated.

Note: As a consequence, when \( \text{vl}=0 \), no elements are updated in the destination vector register group, regardless of \( \text{vstart} \).

The encodings corresponding to the masked versions (\( \text{vm}=0 \)) of \text{vfmv.f.s} and \text{vfmv.s.f} are reserved.

17.3. Vector Slide Instructions

The slide instructions move elements up and down a vector register group.

Note: The slide operations can be implemented much more efficiently than using the arbitrary register gather instruction. Implementations may optimize certain OFFSET values for \( \text{vslideup} \) and \( \text{vslidedown} \). In particular, power-of-2 offsets may operate substantially faster than other offsets.

For all of the \( \text{vslideup} \), \( \text{vslidedown} \), \( \text{v}[f]\text{slide1up} \), and \( \text{v}[f]\text{slide1down} \) instructions, if \( \text{vstart} \geq \text{vl} \), the instruction performs no operation and leaves the destination vector register unchanged.

Note: As a consequence, when \( \text{vl}=0 \), no elements are updated in the destination vector register group, regardless of \( \text{vstart} \).
The tail agnostic/undisturbed policy is followed for tail elements.

The slide instructions may be masked, with mask element $i$ controlling whether destination element $i$ is written. The mask undisturbed/agnostic policy is followed for inactive elements.

### 17.3.1. Vector Slideup Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>vslideup.vx vd, vs2, rs1, vm</code></td>
<td>$vd[i+rs1] = vs2[i]$</td>
</tr>
<tr>
<td><code>vslideup.vi vd, vs2, uimm[4:0], vm</code></td>
<td>$vd[i+uimm] = vs2[i]$</td>
</tr>
</tbody>
</table>

For `vslideup`, the value in $v1$ specifies the maximum number of destination elements that are written. The start index (OFFSET) for the destination can be either specified using an unsigned integer in the x register specified by $rs1$, or a 5-bit immediate, zero-extended to XLEN bits. If XLEN > SEW, OFFSET is not truncated to SEW bits. Destination elements OFFSET through $v1$-1 are written if unmasked and if OFFSET < $v1$.

- `vslideup` behavior for destination elements:
  - OFFSET is amount to slideup, either from x register or a 5-bit immediate
    - $0 < i < \text{max(vstart, OFFSET)}$: Unchanged
    - $\text{max(vstart, OFFSET)} \leq i < v1$: $vd[i] = vs2[i-\text{OFFSET}]$ if v0.mask[i] enabled
    - $v1 \leq i < \text{VLMAX}$: Follow tail policy

The destination vector register group for `vslideup` cannot overlap the source vector register group, otherwise the instruction encoding is reserved.

Note: The non-overlap constraint avoids WAR hazards on the input vectors during execution, and enables restart with non-zero vstart.

### 17.3.2. Vector Slidedown Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>vslidedown.vx vd, vs2, rs1, vm</code></td>
<td>$vd[i] = vs2[i+rs1]$</td>
</tr>
<tr>
<td><code>vslidedown.vi vd, vs2, uimm[4:0], vm</code></td>
<td>$vd[i] = vs2[i+uimm]$</td>
</tr>
</tbody>
</table>

For `vslidedown`, the value in $v1$ specifies the maximum number of destination elements that are written. The remaining elements past $v1$ are handled according to the current tail policy (Section Vector Tail Agnostic and Vector Mask Agnostic vta and vma).

The start index (OFFSET) for the source can be either specified using an unsigned integer in the x register specified by $rs1$, or a 5-bit immediate, zero-extended to XLEN bits. If XLEN > SEW, OFFSET is not truncated to SEW bits.

- `vslidedown` behavior for destination elements for element $i$ in slide:
  - $0 \leq i < \text{vstart}$: Unchanged
  - $\text{vstart} \leq i < v1$: $vd[i] = \text{src}[i]$ if v0.mask[i] enabled
  - $v1 \leq i < \text{VLMAX}$: Follow tail policy

### 17.3.3. Vector Slide1up

Variants of slide are provided that only move by one element but which also allow a scalar integer value to be inserted at the vacated element position.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>vslide1up.vx vd, vs2, rs1, vm</code></td>
<td>$vd[0]=x[rs1]$, $vd[i+1] = vs2[i]$</td>
</tr>
<tr>
<td><code>vfslide1up.vf vd, vs2, rs1, vm</code></td>
<td>$vd[0]=f[rs1]$, $vd[i+1] = vs2[i]$</td>
</tr>
</tbody>
</table>
The vslide1up instruction places the x register argument at location 0 of the destination vector register group, provided that element 0 is active, otherwise the destination element update follows the current mask agnostic/undisturbed policy. If XLEN < SEW, the value is sign-extended to SEW bits. If XLEN > SEW, the least-significant bits are copied over and the high SEW-XLEN bits are ignored.

The remaining active v1-1 elements are copied over from index i in the source vector register group to index i+1 in the destination vector register group.

The v1 register specifies the maximum number of destination vector register elements updated with source values, and remaining elements past v1 are handled according to the current tail policy (Section Vector Tail Agnostic and Vector Mask Agnostic vta and vma).

<table>
<thead>
<tr>
<th>vslide1up behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>i &lt; vstart unchanged</td>
</tr>
<tr>
<td>0 = i = vstart vd[i] = x[rs1] if v0.mask[i] enabled</td>
</tr>
<tr>
<td>max(vstart, 1) &lt;= i &lt; v1 vd[i] = vs2[i-1] if v0.mask[i] enabled</td>
</tr>
<tr>
<td>vl &lt;= i &lt; VLMAX Follow tail policy</td>
</tr>
</tbody>
</table>

The vslide1up instruction requires that the destination vector register group does not overlap the source vector register group. Otherwise, the instruction encoding is reserved.

The vfslide1up instruction is defined analogously, but sources its scalar argument from an f register.

17.3.4. Vector Slide1down Instruction

The vslide1down instruction copies the first v1-1 active elements values from index i+1 in the source vector register group to index i in the destination vector register group.

The v1 register specifies the maximum number of destination vector register elements written with source values, and remaining elements past v1 are handled according to the current tail policy (Section Vector Tail Agnostic and Vector Mask Agnostic vta and vma).

| vslide1down vx vd, vs2, rs1, vm # vd[i] = vs2[i+1], vd[vl-1]=x[rs1] |
| vslide1down vf vd, vs2, rs1, vm # vd[i] = vs2[i+1], vd[vl-1]=f[rs1] |

The vslide1down instruction places the x register argument at location v1-1 in the destination vector register, provided that element v1-1 is active, otherwise the destination element is unchanged. If XLEN < SEW, the value is sign-extended to SEW bits. If XLEN > SEW, the least-significant bits are copied over and the high SEW-XLEN bits are ignored.

<table>
<thead>
<tr>
<th>vslide1down behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>i &lt; vstart unchanged</td>
</tr>
<tr>
<td>vstart &lt;= i &lt; v1-1 vd[i] = vs2[i+1] if v0.mask[i] enabled</td>
</tr>
<tr>
<td>vstart &lt;= i = v1-1 vd[v1-1] = x[rs1] if v0.mask[i] enabled</td>
</tr>
<tr>
<td>vl &lt;= i &lt; VLMAX Follow tail policy</td>
</tr>
</tbody>
</table>

The vfslide1down instruction is defined analogously, but sources its scalar argument from an f register.

Note

The vslide1down instruction can be used to load values into a vector register without using memory and without disturbing other vector registers. This provides a path for debuggers to modify the contents of a vector register, albeit slowly, with multiple repeated vslide1down invocations.

17.4. Vector Register Gather Instructions

The vector register gather instructions read elements from a first source vector register group at locations given by a second source vector register group. The index values in the second vector are treated as unsigned integers. The source vector can be read at any index < VLMAX regardless of v1. The maximum number of elements to write to the destination register is given by v1, and the remaining elements past v1 are handled according to the current tail policy (Section Vector Tail Agnostic
and Vector Mask Agnostic vta and vma). The operation can be masked, and the mask undisturbed/agnostic policy is followed for inactive elements.

\[
vrgather.vv \ vd, \ vs2, \ vs1, \ vm \ # \ vd[i] = (vs1[i] >= VLMAX) ? 0 : vs2[vs1[i]];
\]

\[
vrgatherei16.vv \ vd, \ vs2, \ vs1, \ vm \ # \ vd[i] = (vs1[i] >= VLMAX) ? 0 : vs2[vs1[i]];
\]

The \textit{vrgather} . \textit{vv} form uses SEW/LMUL for both the data and indices. The \textit{vrgatherei16} . \textit{vv} form uses SEW/LMUL for the data in \textit{vs2} but EEW=16 and EMUL = (16/SEW)*LMUL for the indices in \textit{vs1}.

\begin{itemize}
  \item When SEW=8, \textit{vrgather} . \textit{vv} can only reference vector elements 0-255. The \textit{vrgatherei16} form can index 64K elements, and can also be used to reduce the register capacity needed to hold indices when SEW > 16.
\end{itemize}

If an element index is out of range (\textit{vs1[i]} \geq VLMAX) then zero is returned for the element value.

Vector-scalar and vector-immediate forms of the register gather are also provided. These read one element from the source vector at the given index, and write this value to the active elements at the start of the destination vector register. The index value in the scalar register and the immediate, zero-extended to XLEN bits, are treated as unsigned integers. If XLEN > SEW, the index value is \textit{not} truncated to SEW bits.

\begin{itemize}
  \item These forms allow any vector element to be “splatted” to an entire vector.
\end{itemize}

\[
vrgather.vx \ vd, \ vs2, \ rs1, \ vm \ # \ vd[i] = (x[rs1] >= VLMAX) ? 0 : vs2[x[rs1]]
\]

\[
vrgather.vi \ vd, \ vs2, \ uimm, \ vm \ # \ vd[i] = (uimm >= VLMAX) ? 0 : vs2[uimm]
\]

For any \textit{vrgather} instruction, the destination vector register group cannot overlap with the source vector register groups, otherwise the instruction encoding is reserved.

### 17.5. Vector Compress Instruction

The vector compress instruction allows elements selected by a vector mask register from a source vector register group to be packed into contiguous elements at the start of the destination vector register group.

\[
vcompress.vm \ vd, \ vs2, \ vs1 \ # \ Compress \ into \ vd \ elements \ of \ vs2 \ where \ vs1 \ is \ enabled
\]

The vector mask register specified by \textit{vs1} indicates which of the first \textit{v1} elements of vector register group \textit{vs2} should be extracted and packed into contiguous elements at the beginning of vector register \textit{vd}. The remaining elements of \textit{vd} are treated as tail elements according to the current tail policy (Section \textit{Vector Tail Agnostic} and \textit{Vector Mask Agnostic vta and vma}).

\[
\begin{array}{c}
110100101 \ v0
\end{array}
\]

\[
\begin{array}{c}
876543210 \ v1
\end{array}
\]

\[
\begin{array}{c}
123456789 \ v2
\end{array}
\]

\[
vcompress.vm \ v2, \ v1, \ v0
\]

\[
\begin{array}{c}
123487520 \ v2
\end{array}
\]

\textit{vcompress} is encoded as an unmasked instruction (\textit{vm}=1). The equivalent masked instruction (\textit{vm}=0) is reserved.

The destination vector register group cannot overlap the source vector register group or the source mask register, otherwise the instruction encoding is reserved.

A trap on a \textit{vcompress} instruction is always reported with a \textit{vstart} of 0. Executing a \textit{vcompress} instruction with a non-zero \textit{vstart} raises an illegal instruction exception.

\begin{itemize}
  \item Although possible, \textit{vcompress} is one of the more difficult instructions to restart with a non-zero \textit{vstart}, so assumption is implementations will choose not do that but will instead restart from element 0. This does mean elements in destination register after \textit{vstart} will already have been updated.
\end{itemize}
17.5.1. Synthesizing \texttt{vdecompress}

There is no inverse \texttt{vdecompress} provided, as this operation can be readily synthesized using \texttt{iota} and a masked \texttt{vrgather}:

\begin{verbatim}
Desired functionality of 'vdecompress'
7 6 5 4 3 2 1 0     # vid
e d c b a     # packed vector of 5 elements
1 0 0 1 1 1 0 1     # mask vector of 8 elements
p q r s t u v w     # destination register before vdecompress

e q r d c b v a     # result of vdecompress
\end{verbatim}

\begin{verbatim}
# v0 holds mask
# v1 holds packed data
# v11 holds input expanded vector and result
\texttt{viota.m v10, v0}                # Calc \texttt{iota} from mask in v0
\texttt{vrgather.vv v11, v1, v10, v0.t} # Expand into destination
\end{verbatim}

\begin{verbatim}
p q r s t u v w     # v11 destination register
e d c b a     # v1 source vector
1 0 0 1 1 1 0 1     # v0 mask vector
4 4 4 3 2 1 1 0     # v10 result of \texttt{viota.m}
e q r d c b v a     # v11 destination after \texttt{vrgather} using \texttt{viota.m} under mask
\end{verbatim}

17.6. Whole Vector Register Move

The \texttt{vmv\<nr>r.v} instructions copy whole vector registers (i.e., all VLEN bits) and can copy whole vector register groups. The instructions operate as if EEW=SEW, EMUL = \texttt{nr}, effective length \texttt{evl} = EMUL * VLEN/SEW.

\begin{verbatim}
vmv<nr>r.v vd, vs2  # General form

vmv1r.v v1, v2     # Copy v1=v2
vmv2r.v v10, v12    # Copy v10=v12; v11=v13
vmv4r.v v4, v8      # Copy v4=v8; v5=v9; v6=v10; v7=v11
vmv8r.v v0, v8      # Copy v0=v8; v1=v9; ...; v7=v15
\end{verbatim}

The source and destination vector register numbers must be aligned appropriately for the vector register group size, and encodings with other vector register numbers are reserved.

\begin{verbatim}
Note A future extension may support other numbers of registers to be moved. Values of \texttt{simm} other than 0, 1, 3, and 7 are currently reserved.
Note The instruction uses the same \texttt{funct6} encoding as the \texttt{vsmul} instruction but with an immediate operand, and only the unmasked version (\texttt{vm}=1). This encoding is chosen as it is close to the related \texttt{vmerge} encoding, and it is unlikely the \texttt{vsmul} instruction would benefit from an immediate form.
\end{verbatim}
18. Exception Handling

On a trap during a vector instruction (caused by either a synchronous exception or an asynchronous interrupt), the existing *epc CSR is written with a pointer to the errant vector instruction, while the vstart CSR contains the element index that caused the trap to be taken.

**Note**
We chose to add a vstart CSR to allow resumption of a partially executed vector instruction to reduce interrupt latencies and to simplify forward-progress guarantees. This is similar to the scheme in the IBM 3090 vector facility. To ensure forward progress without the vstart CSR, implementations would have to guarantee an entire vector instruction can always complete atomically without generating a trap. This is particularly difficult to ensure in the presence of strided or scatter/gather operations and demand-paged virtual memory.

18.1. Precise vector traps

**Note**
We assume most supervisor-mode environments with demand-paging will require precise vector traps.

Precise vector traps require that:

1. all instructions older than the trapping vector instruction have committed their results
2. no instructions newer than the trapping vector instruction have altered architectural state
3. any operations within the trapping vector instruction affecting result elements preceding the index in the vstart CSR have committed their results
4. no operations within the trapping vector instruction affecting elements at or following the vstart CSR have altered architectural state except if restarting and completing the affected vector instruction will nevertheless produce the correct final state.

We relax the last requirement to allow elements following vstart to have been updated at the time the trap is reported, provided that re-executing the instruction from the given vstart will correctly overwrite those elements.

In idempotent memory regions, vector store instructions may have updated elements in memory past the element causing a synchronous trap. Non-idempotent memory regions must not have been updated for indices equal to or greater than the element that caused a synchronous trap during a vector store instruction.

Except where noted above, vector instructions are allowed to overwrite their inputs, and so in most cases, the vector instruction restart must be from the vstart location. However, there are a number of cases where this overwrite is prohibited to enable execution of the vector instructions to be idempotent and hence restartable from any location.

Implementations must ensure forward progress can be eventually guaranteed for the element or segment reported by vstart.

18.2. Imprecise vector traps

Imprecise vector traps are traps that are not precise. In particular, instructions newer than *epc may have committed results, and instructions older than *epc may have not completed execution. Imprecise traps are primarily intended to be used in situations where reporting an error and terminating execution is the appropriate response.

**Note**
A profile might specify that interrupts are precise while other traps are imprecise. We assume many embedded implementations will generate only imprecise traps for vector instructions on fatal errors, as they will not require resumable traps.

Imprecise traps shall report the faulting element in vstart for traps caused by synchronous vector exceptions.

18.3. Selectable precise/imprecise traps

Some profiles may choose to provide a privileged mode bit to select between precise and imprecise vector traps. Imprecise mode would run at high-performance but possibly make it difficult to discern error causes, while precise mode would run more slowly, but support debugging of errors albeit with a possibility of not experiencing the same errors as in imprecise mode.
18.4. Swappable traps

Another trap mode can support swappable state in the vector unit, where on a trap, special instructions can save and restore the vector unit microarchitectural state, to allow execution to continue correctly around imprecise traps.

This mechanism is not defined in the base vector ISA.

Note | A future extension might define a standard way of saving and restoring opaque microarchitectural state from a vector unit implementation to support context switching with imprecise traps.
## 19. Vector Instruction Listing

<table>
<thead>
<tr>
<th>Integer</th>
<th>Integer</th>
<th>FP</th>
</tr>
</thead>
<tbody>
<tr>
<td>funct3</td>
<td>funct3</td>
<td>funct3</td>
</tr>
<tr>
<td>OPIVV</td>
<td>OPMVV</td>
<td>OPFVV</td>
</tr>
<tr>
<td>OPIVX</td>
<td>OPMVX</td>
<td>OPFVF</td>
</tr>
<tr>
<td>OPIVI</td>
<td></td>
<td>I</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>funct6</th>
<th>funct6</th>
<th>funct6</th>
</tr>
</thead>
<tbody>
<tr>
<td>000000 V X I vadd</td>
<td>000000 V vredsum</td>
<td>000000 V F vfadd</td>
</tr>
<tr>
<td>000010 V X vsub</td>
<td>000010 V vredor</td>
<td>000010 V F vsub</td>
</tr>
<tr>
<td>000011 X I vrsb</td>
<td>000011 V vredxor</td>
<td>000011 V F vfredsum</td>
</tr>
<tr>
<td>000100 V X vmin</td>
<td>000100 V vredminu</td>
<td>000100 V F vmin</td>
</tr>
<tr>
<td>000101 V X vmin</td>
<td>000101 V vredmin</td>
<td>000101 V F vfredmin</td>
</tr>
<tr>
<td>000110 V X vmaxu</td>
<td>000110 V vredmaxu</td>
<td>000110 V F vmax</td>
</tr>
<tr>
<td>000111 V X vmax</td>
<td>000111 V vredmax</td>
<td>000111 V F vfredmax</td>
</tr>
<tr>
<td>001000</td>
<td>001000 V X vaadd</td>
<td>001000 V F vfsnij</td>
</tr>
<tr>
<td>001001 V X I vand</td>
<td>001001 V X vaadd</td>
<td>001001 V F vfsnij</td>
</tr>
<tr>
<td>001010 V X I vor</td>
<td>001010 V X vasubu</td>
<td>001010 V F vfsnijx</td>
</tr>
<tr>
<td>001011 V X I vxor</td>
<td>001011 V X vasub</td>
<td>001011</td>
</tr>
<tr>
<td>001100 V X I vrgather</td>
<td>001100</td>
<td>001100</td>
</tr>
<tr>
<td>001101</td>
<td>001101</td>
<td></td>
</tr>
<tr>
<td>001110 X I vslideup</td>
<td>001110 X vslide1up</td>
<td>001110 F vfslide1up</td>
</tr>
<tr>
<td>001110 V vrgatherei16</td>
<td></td>
<td></td>
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Table 19. VRXUNARY0 encoding space

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Table 20. VWXUNARY0 encoding space

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Table 21. VXUNARY0 encoding space

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Table 22. VRFUNARY0 encoding space

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Appendix A: Vector Assembly Code Examples

The following are provided as non-normative text to help explain the vector ISA.

A.1. Vector-vector add example

```assembly
# vector-vector add routine of 32-bit integers
# void vvaddint32(size_t n, const int*x, const int*y, int*z)
# { for (size_t i=0; i<n; i++) { z[i]=x[i]+y[i]; } }
#
# a0 = n, a1 = x, a2 = y, a3 = z
# Non-vector instructions are indented
vvaddint32:
  vsetvli t0, a0, e32, ta, ma  # Set vector length based on 32-bit vectors
  vle32.v v0, (a1)         # Get first vector
  sub a0, a0, t0         # Decrement number done
  slli t0, t0, 2         # Multiply number done by 4 bytes
  add a1, a1, t0         # Bump pointer
  vle32.v v1, (a2)         # Get second vector
  add a2, a2, t0         # Bump pointer
  vadd.vv v2, v0, v1       # Sum vectors
  vse32.v v2, (a3)         # Store result
  add a3, a3, t0         # Bump pointer
  bnez a0, vvaddint32    # Loop back
  ret                    # Finished
```

A.2. Example with mixed-width mask and compute.

```assembly
# Code using one width for predicate and different width for masked
# compute.
#   int8_t a[], int32_t b[], c[];
#   for (i=0; i<n; i++) { b[i] =  (a[i] < 5) ? c[i] : 1; }
#
# Mixed-width code that keeps SEW/LMUL=8
loop:
  vsetvli a4, a0, e8, m1, ta, ma  # Byte vector for predicate calc
  vle8.v v1, (a1)                  # Load a[i]
  add a1, a1, a4                   # Bump pointer.
  vmvlt.vi v0, v1, 5               # a[i] < 5?
  vsetvli x0, a0, e32, m4, ta, mu # Vector of 32-bit values.
  sub a0, a0, a4                   # Decrement count
  vmv.v.i v4, 1                    # Splat immediate to destination
  vle32.v v4, (a3), v0.t           # Load requested elements of C, others undisturbed
  sll t1, t1, 2                    # Bump pointer.
  vse32.v v4, (a2)                 # Store b[i].
  add a2, a2, t1                   # Bump pointer.
  bnez a0, loop                    # Any more?
```

A.3. Memcpy example
# void *memcpy(void* dest, const void* src, size_t n)
# a0=dest, a1=src, a2=n
#
memcpy:
    mv a3, a0 # Copy destination
loop:
    vsetvli t0, a2, e8,m8,ta,ma # Vectors of 8b
    vle8.v v0, (a1) # Load bytes
    add a1, a1, t0 # Bump pointer
    sub a2, a2, t0 # Decrement count
    vse8.v v0, (a3) # Store bytes
    add a3, a3, t0 # Bump pointer
    bnez a2, loop # Any more?
    ret # Return

A.4. Conditional example

# (int16) z[i] = ((int8) x[i] < 5) ? (int16) a[i] : (int16) b[i];
#
loop:
    vsetvli t0, a0, e8,m1,ta,ma # Use 8b elements.
    vle8.v v0, (a1) # Get x[i]
    sub a0, a0, t0 # Decrement element count
    add a1, a1, t0 # x[i] Bump pointer
    vmslt.vi v0, 5 # Set mask in v0
    vsetvli t0, a0, e16,m2,ta,mu # Use 16b elements.
    slli t0, t0, 1 # Multiply by 2 bytes
    vle16.v v2, (a2), v0.t # z[i] = a[i] case
    vmnot.m v0, v0 # Invert v0
    add a2, a2, t0 # a[i] bump pointer
    vle16.v v2, (a3), v0.t # z[i] = b[i] case
    add a3, a3, t0 # b[i] bump pointer
    vse16.v v2, (a4) # Store z
    add a4, a4, t0 # z[i] bump pointer
    bnez a2, loop

A.5. SAXPY example
A.6. SGEMM example
# RV64IDV system
#
# void
# sgemm_nn(size_t n,
#          size_t m,
#          size_t k,
#          const float*a,   // m * k matrix
#          size_t lda,
#          const float*b,   // k * n matrix
#          size_t ldb,
#          float*c,         // m * n matrix
#          size_t ldc)
#
#  c += a*b (alpha=1, no transpose on input matrices)
#  matrices stored in C row-major order

#define n a0
#define m a1
#define k a2
#define ap a3
#define astride a4
#define bp a5
#define bstride a6
#define cp a7
#define cstride t0
#define kt t1
#define nt t2
#define bnp t3
#define cnp t4
#define akp t5
#define bkp s0
#define nvl s1
#define ccp s2
#define amp s3

# Use args as additional temporaries
#define ft12 fa0
#define ft13 fa1
#define ft14 fa2
#define ft15 fa3

# This version holds a 16*VLMAX block of C matrix in vector registers
# in inner loop, but otherwise does not cache or TLB tiling.

sgemm_nn:
    addi sp, sp, -FRAMESIZE
    sd s0, OFFSET(sp)
    sd s1, OFFSET(sp)
    sd s2, OFFSET(sp)

    # Check for zero size matrices
    beqz n, exit
    beqz m, exit
    beqz k, exit

    # Convert elements strides to byte strides.
    ld cstride, OFFSET(sp)  # Get arg from stack frame
    slli astride, astride, 2
    slli bstride, bstride, 2
    slli cstride, cstride, 2

    slti t6, m, 16
    bnez t6, end_rows
c_row_loop: # Loop across rows of C blocks
    mv nt, n  # Initialize n counter for next row of C blocks
    mv bnp, bp # Initialize B n-loop pointer to start
    mv cnp, cp # Initialize C n-loop pointer

c_col_loop: # Loop across one row of C blocks
    vsetvli nvl, nt, e32, ta, ma  # 32-bit vectors, LMUL=1
    mv akp, ap   # reset pointer into A to beginning
    mv bkp, bnp # step to next column in B matrix
    # Initialize current C submatrix block from memory.
    vle32.v  v0, (cnp); add ccp, cnp, cstride;
    vle32.v  v1, (ccp); add ccp, ccp, cstride;
    vle32.v  v2, (ccp); add ccp, ccp, cstride;
    vle32.v  v3, (ccp); add ccp, ccp, cstride;
    vle32.v  v4, (ccp); add ccp, ccp, cstride;
    vle32.v  v5, (ccp); add ccp, ccp, cstride;
    vle32.v  v6, (ccp); add ccp, ccp, cstride;
    vle32.v  v7, (ccp); add ccp, ccp, cstride;
    vle32.v  v8, (ccp); add ccp, ccp, cstride;
    vle32.v  v9, (ccp); add ccp, ccp, cstride;
    vle32.v v10, (ccp); add ccp, ccp, cstride;
    vle32.v v11, (ccp); add ccp, ccp, cstride;
    vle32.v v12, (ccp); add ccp, ccp, cstride;
    vle32.v v13, (ccp); add ccp, ccp, cstride;
    vle32.v v14, (ccp); add ccp, ccp, cstride;
    vle32.v v15, (ccp)

    mv kt, k # Initialize inner loop counter

    # Inner loop scheduled assuming 4-clock occupancy of vfmacc instruction and single-issue pipeline
    # Software pipeline loads
    flw ft0, (akp); add amp, akp, astride;
    flw ft1, (amp); add amp, amp, astride;
    flw ft2, (amp); add amp, amp, astride;
    flw ft3, (amp); add amp, amp, astride;
    # Get vector from B matrix
    vle32.v v16, (bkp)

    # Loop on inner dimension for current C block
    k_loop:
        vfmacc.vf v0, ft0, v16
        add bkp, bkp, bstride
        flw ft4, (amp)
        add amp, amp, astride
        vfmacc.vf v1, ft1, v16
        addi kt, kt, -1  # Decrement k counter
        flw ft5, (amp)
        add amp, amp, astride
        vfmacc.vf v2, ft2, v16
        flw ft6, (amp)
        add amp, amp, astride
        vfmacc.vf v3, ft3, v16
        add amp, amp, astride
        flw ft8, (amp)
        add amp, amp, astride
        vfmacc.vf v4, ft4, v16
        flw ft9, (amp)
add amp, amp, astride
vfmacc.vf v5, ft5, v16
flw ft10, (amp)
add amp, amp, astride
vfmacc.vf v6, ft6, v16
flw ft11, (amp)
add amp, amp, astride
vfmacc.vf v7, ft7, v16
flw ft12, (amp)
add amp, amp, astride
vfmacc.vf v8, ft8, v16
flw ft13, (amp)
add amp, amp, astride
vfmacc.vf v9, ft9, v16
flw ft14, (amp)
add amp, amp, astride
vfmacc.vf v10, ft10, v16
flw ft15, (amp)
add amp, amp, astride
addi akp, akp, 4            # Move to next column of a
vfmacc.vf v11, ft11, v16
beqz kt, 1f                 # Don't load past end of matrix
flw ft0, (akp)
add amp, akp, astride
1:  vfmacc.vf v12, ft12, v16
1:  vfmacc.vf v13, ft13, v16
1:  vfmacc.vf v14, ft14, v16
beqz kt, 1f                 # Exit out of loop
flw ft1, (amp)
add amp, amp, astride
flw ft2, (amp)
add amp, amp, astride
flw ft3, (amp)
add amp, amp, astride
vfmacc.vf v15, ft15, v16
vle32.v v16, (bkp)            # Get next vector from B matrix, overlap loads with jump stalls
j k_loop

1:  vfmacc.vf v15, ft15, v16

# Save C matrix block back to memory
vse32.v v0, (cnp); add ccp, cnp, cstride;
vse32.v v1, (ccp); add ccp, cnp, cstride;
vse32.v v2, (ccp); add ccp, CCP, cstride;
vse32.v v3, (ccp); add CCP, CCP, cstride;
vse32.v v4, (ccp); add CCP, CCP, cstride;
vse32.v v5, (ccp); add CCP, CCP, cstride;
vse32.v v6, (ccp); add CCP, CCP, cstride;
vse32.v v7, (ccp); add CCP, CCP, cstride;
vse32.v v8, (ccp); add CCP, CCP, cstride;
vse32.v v9, (ccp); add CCP, CCP, cstride;
vse32.v v10, (ccp); add CCP, CCP, cstride;
vse32.v v11, (ccp); add CCP, CCP, cstride;
vse32.v v12, (ccp); add CCP, CCP, cstride;
vse32.v v13, (ccp); add CCP, CCP, cstride;
vse32.v v14, (ccp); add CCP, CCP, cstride;
vse32.v v15, (ccp)

# Following tail instructions should be scheduled earlier in free slots during C block save.
# Leaving here for clarity.
# Bump pointers for loop across blocks in one row
A.7. Division approximation example

# v1 = v1 / v2 to almost 23 bits of precision.

vfmul.vv v3, v3, v4          # Better estimate of 1/v2
vfmul.vv v1, v1, v3          # Estimate of v1/v2

A.8. Square root approximation example
# v1 = sqrt(v1) to almost 23 bits of precision.

    fmv.w.x ft0, x0       # Mask off zero inputs
vmfne.vf v0, v1, ft0    # to avoid div by zero
vfrsqrt7.v v2, v1, v0.t  # Estimate 1/sqrt(x)
vmfne.vf v0, v2, ft0, v0.t  # Additionally mask off +inf inputs
    li t0, 0xbf000000
    fmv.w.x ft0, t0       # -0.5
vmfadd.vf v3, v1, ft0, v0.t  # -0.5 * x
vmfadd.vv v4, v2, v2, v0.t  # est * est
    li t0, 0x3fc00000
vmfadd.vv v5, t0, v0.t    # Splat 1.5
vmfadd.vv v4, v3, v5, v0.t  # 1.5 - 0.5 * x * est * est
vmfadd.vv v1, v1, v4, v0.t  # estimate to 14 bits
vmfadd.vv v4, v1, v1, v0.t  # est * est
vmfadd.vv v4, v3, v5, v0.t  # 1.5 - 0.5 * x * est * est
vmfadd.vv v1, v1, v4, v0.t  # estimate to 23 bits

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Appendix B: Calling Convention

In the RISC-V psABI, the vector registers v0-v31 are all caller-saved. The v1 and vtype CSRs are also caller-saved.

Procedures may assume that vstart is zero upon entry. Procedures may assume that vstart is zero upon return from a procedure call.

Note Application software should normally not write vstart explicitly. Any procedure that does explicitly write vstart to a nonzero value must zero vstart before either returning or calling another procedure.

The vxrm and vxsat fields of vcsr have thread storage duration.

Executing a system call causes all caller-saved vector registers (v0-v31, v1, vtype) and vstart to become unspecified.

Note This scheme allows system calls that cause context switches to avoid saving and later restoring the vector registers.

Note Most OSes will choose to either leave these registers intact or reset them to their initial state to avoid leaking information across process boundaries.
Appendix C: Vector Quad-Widening Integer Multiply-Add Instructions (Extension Zvqmac)

Note This is only a proposal for a future extension after v1.0 and might change substantially before ratification.

The quad-widening integer multiply-add instructions add a SEW-bit*SEW-bit multiply result to (from) a 4*SEW-bit value and produce a 4*SEW-bit result. All combinations of signed and unsigned multiply operands are supported.

Note These instructions are currently not planned to be part of the base V extension.

Note On ELEN=32 machines, only 8b * 8b = 16b products accumulated in a 32b accumulator would be supported. Machines with ELEN=64 would also add 16b * 16b = 32b products accumulated in 64b.

# Quad-widening unsigned-integer multiply-add, overwrite addend
vqmaccu.vv vd, vs1, vs2, vm    # vd[i] = +(vs1[i] * vs2[i]) + vd[i]
vqmaccu.vx vd, rs1, vs2, vm    # vd[i] = +(x[rs1] * vs2[i]) + vd[i]

# Quad-widening signed-integer multiply-add, overwrite addend
vqmacc.vv vd, vs1, vs2, vm    # vd[i] = +(vs1[i] * vs2[i]) + vd[i]
vqmacc.vx vd, rs1, vs2, vm    # vd[i] = +(x[rs1] * vs2[i]) + vd[i]

# Quad-widening signed-unsigned-integer multiply-add, overwrite addend
vqmaccsu.vv vd, vs1, vs2, vm    # vd[i] = +(signed(vs1[i]) * unsigned(vs2[i])) + vd[i]
vqmaccsus.vx vd, rs1, vs2, vm    # vd[i] = +(signed(x[rs1]) * unsigned(vs2[i])) + vd[i]

# Quad-widening unsigned-signed-integer multiply-add, overwrite addend
vqmaccus.vx vd, rs1, vs2, vm    # vd[i] = +(unsigned(x[rs1]) * signed(vs2[i])) + vd[i]
Appendix D: Divided Element Extension (Extension Zvediv)

The EDIV extension is currently not planned to be part of the base "V" extension, and will change substantially from this current sketch.

This section has not been updated to account for new mask format in v0.9.

The divided element extension allows each element to be treated as a packed sub-vector of narrower elements. This provides efficient support for some forms of narrow-width and mixed-width arithmetic, and also to allow outer-loop vectorization of short vector and matrix operations. In addition to modifying the behavior of some existing instructions, a few new instructions are provided to operate on vectors when EDIV > 1.

The divided element extension adds a two-bit field, vdiv[1:0] to the vtype register.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XLEN-1</td>
<td>vill</td>
<td>Illegal value if set</td>
</tr>
<tr>
<td>XLEN-2:10</td>
<td>vdiv[1:0]</td>
<td>Reserved (write 0)</td>
</tr>
<tr>
<td>9:8</td>
<td>vdiv[1:0]</td>
<td>Used by EDIV extension</td>
</tr>
<tr>
<td>7</td>
<td>vma</td>
<td>Mask agnostic</td>
</tr>
<tr>
<td>6</td>
<td>vta</td>
<td>Tail agnostic</td>
</tr>
<tr>
<td>5:3</td>
<td>vsew[2:0]</td>
<td>Selected element width (SEW) setting</td>
</tr>
<tr>
<td>2:0</td>
<td>vlmul[2:0]</td>
<td>Vector register group multiplier (LMUL) setting</td>
</tr>
</tbody>
</table>

The vdiv field encodes the number of ways, EDIV, into which each SEW-bit element is subdivided into equal sub-elements. A vector register group is now considered to hold a vector of sub-vectors.

<table>
<thead>
<tr>
<th>vdiv[1:0]</th>
<th>Division EDIV</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>1 (undivided, as in base)</td>
</tr>
<tr>
<td>0 1</td>
<td>2 two equal sub-elements</td>
</tr>
<tr>
<td>1 0</td>
<td>4 four equal sub-elements</td>
</tr>
<tr>
<td>1 1</td>
<td>8 eight equal sub-elements</td>
</tr>
</tbody>
</table>

The assembly syntax for vsetvli has additional options added to encode the EDIV options.

```
d1   # EDIV 1, assumed if d setting absent
d2   # EDIV 2
d4   # EDIV 4
d8   # EDIV 8
vsetvli t0, a0, e32,m2,d4   # SEW=32, LMUL=2, EDIV=4
```
<table>
<thead>
<tr>
<th>SEW</th>
<th>EDIV</th>
<th>Sub-element</th>
<th>Integer accumulator</th>
<th>FP sum/dot accumulator</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>sum</td>
<td>dot</td>
</tr>
<tr>
<td>8b</td>
<td>2</td>
<td>4b</td>
<td>8b</td>
<td>8b</td>
</tr>
<tr>
<td>8b</td>
<td>4</td>
<td>2b</td>
<td>8b</td>
<td>8b</td>
</tr>
<tr>
<td>8b</td>
<td>8</td>
<td>1b</td>
<td>8b</td>
<td>8b</td>
</tr>
<tr>
<td>16b</td>
<td>2</td>
<td>8b</td>
<td>16b</td>
<td>16b</td>
</tr>
<tr>
<td>16b</td>
<td>4</td>
<td>8b</td>
<td>16b</td>
<td>8b</td>
</tr>
<tr>
<td>32b</td>
<td>2</td>
<td>16b</td>
<td>32b</td>
<td>32b</td>
</tr>
<tr>
<td>32b</td>
<td>4</td>
<td>8b</td>
<td>16b</td>
<td>32b</td>
</tr>
<tr>
<td>32b</td>
<td>8</td>
<td>4b</td>
<td>8b</td>
<td>8b</td>
</tr>
<tr>
<td>64b</td>
<td>2</td>
<td>32b</td>
<td>64b</td>
<td>64b</td>
</tr>
<tr>
<td>64b</td>
<td>4</td>
<td>16b</td>
<td>32b</td>
<td>64b</td>
</tr>
<tr>
<td>64b</td>
<td>8</td>
<td>8b</td>
<td>16b</td>
<td>32b</td>
</tr>
<tr>
<td>128b</td>
<td>2</td>
<td>64b</td>
<td>128b</td>
<td>32b</td>
</tr>
<tr>
<td>128b</td>
<td>4</td>
<td>32b</td>
<td>64b</td>
<td>128b</td>
</tr>
<tr>
<td>128b</td>
<td>8</td>
<td>16b</td>
<td>32b</td>
<td>64b</td>
</tr>
<tr>
<td>256b</td>
<td>2</td>
<td>128b</td>
<td>256b</td>
<td>256b</td>
</tr>
<tr>
<td>256b</td>
<td>4</td>
<td>64b</td>
<td>128b</td>
<td>256b</td>
</tr>
<tr>
<td>256b</td>
<td>8</td>
<td>32b</td>
<td>64b</td>
<td>128b</td>
</tr>
</tbody>
</table>

Each implementation defines a minimum size for a sub-element, \( SELEN \), which must be at most 8 bits.

**Note** While \( SELEN \) is a fourth implementation-specific parameter, values smaller than 8 would be considered an additional extension.

### D.1. Instructions not affected by EDIV

The vector start register \( vstart \) and exception reporting continue to work as before.

The vector length \( vl \) control and vector masking continue to operate at the element level.

Vector masking continues to operate at the element level, so sub-elements cannot be individually masked.

**Note** SEW can be changed dynamically to enabled per-element masking for sub-elements of 8 bits and greater.

Vector load/store and AMO instructions are unaffected by EDIV, and continue to move whole elements.

Vector mask logical operations are unchanged by EDIV setting, and continue to operate on vector registers containing element masks.

Vector mask population count (\( vpopc \)), find-first and related instructions (\( vfirst, vmsbf, vmsif, vmsof \)), iota (\( viota \)), and element index (\( vid \)) instructions are unaffected by EDIV.

Vector integer bit insert/extract, and integer and floating-point scalar move instruction are unaffected by EDIV.

Vector slide-up/slide-down are unaffected by EDIV.

Vector compress instructions are unaffected by EDIV.

### D.2. Instructions Affected by EDIV

#### D.2.1. Regular Vector Arithmetic Instructions under EDIV

Most vector arithmetic operations are modified to operate on the individual sub-elements, so effective SEW is SEW/EDIV and effective vector length is \( vl \times EDIV \). For example, a vector add of 32-bit elements with a \( vl \) of 5 and EDIV of 4, operates...
identically to a vector add of 8-bit elements with a vector length of 20.

```
vsetvli t0, a0, e32,m1,d4  # Vectors of 32-bit elements, divided into byte sub-elements
vadd.vv v1,v2,v3          # Performs a vector of 4*vl 8-bit additions.
vsll.vx v1,v2,x1           # Performs a vector of 4*vl 8-bit shifts.
```

D.2.2. Vector Add with Carry/Subtract with Borrow Reserved under EDIV>1

For EDIV > 1, vadc, vmadc, vsbc, vmsbc are reserved.

D.2.3. Vector Reduction Instructions under EDIV

Vector single-width integer sum reduction instructions are reserved under EDIV>1. Other vector single-width reductions and vector widening integer sum reduction instructions now operate independently on all elements in a vector, reducing sub-element values within an element to an element-wide result.

The scalar input is taken from the least-significant bits of the second operand, with the number of bits equal to the number of significant result bits (i.e., for sum and dot reductions, the number of bits are given in table above, for non-sum and non-dot reductions, equal to the element size).

```
# Sum each sub-vector of four bytes into a 16-bit result.
vsetvli t0, a0, e32,d4  # Vectors of 32-bit elements, divided into byte sub-elements
vwredsum.vs v1, v2, v3 # v1[i][15:0] = v2[i][31:24] + v2[i][23:16]
 #              + v2[i][15:8] + v2[i][7:0] + v3[i][15:0]

# Find maximum among sub-elements
vredmax.vs v5, v6, v7 # v5[i][7:0] = max(v6[i][31:24], v6[i][23:16],
 #                    v6[i][15:8], v6[i][7:0], v7[i][7:0])
```

Integer sub-element non-sum reductions produce a final result that is max(8,SEW/EDIV) bits wide, sign- or zero-extended to full SEW if necessary.

Integer sub-element widening sum reductions produce a final result that is max(8,min(SEW,2*SEW/EDIV)) bits wide, sign- or zero-extended to full SEW if necessary.

Single-width floating-point reductions produce a final result that is SEW/EDIV bits wide.

Widening floating-point sum reductions produce a final result that is min(2*SEW/EDIV,FLEN) bits wide, NaN-boxed to the full SEW width if necessary.

D.2.4. Vector Register Gather Instructions under EDIV

Vector register gather instructions under non-zero EDIV only gather sub-elements within the element. The source and index values are interpreted as relative to the enclosing element only. Index values ≥ EDIV write a zero value into the result sub-element.

```
|       |       |  SEW = 32b, EDIV=4
7 6 5 4 3 2 1 0  | bytes
  d e a d b e e f  | v1
  0 1 9 2 0 2 3 2  | v2
  d a 0 e f e b e  | v3
vrgather.vv v3, v1, v2
vrgather.vi v4, v1, 1
```

Note: Vector register gathers with scalar or immediate arguments can "splat" values across sub-elements within an element.

Note: Implementations can provide fast implementations of register gathers constrained within a single element width.
D.3. Vector Integer Dot-Product Instruction

The integer dot-product reduction `vdot.vv` performs an element-wise multiplication between the source sub-elements then accumulates the results into the destination vector element. Note the assembler syntax uses a `.vv` suffix since both inputs are vectors of elements.

Sub-element integer dot reductions produce a final result that is `max(8,min(SEW,4*SEW/EDIV))` bits wide, sign- or zero-extended to full SEW if necessary.

```assembly
# Unsigned dot-product
vdotu.vv vd, vs2, vs1, vm  # Vector-vector

# Signed dot-product
vdot.vv vd, vs2, vs1, vm  # Vector-vector
```

```
# Dot product, SEW=32, EDIV=1
vdot.vv vd, vs2, vs1, vm  # vd[i][31:0] += vs2[i][31:0] * vs1[i][31:0]

# Dot product, SEW=32, EDIV=2
vdot.vv vd, vs2, vs1, vm  # vd[i][31:0] += vs2[i][31:16] * vs1[i][31:16] + vs2[i][15:0] * vs1[i][15:0]

# Dot product, SEW=32, EDIV=4
```

D.4. Vector Floating-Point Dot Product Instruction

The floating-point dot-product reduction `vfdot.vv` performs an element-wise multiplication between the source sub-elements then accumulates the results into the destination vector element. Note the assembler syntax uses a `.vv` suffix since both inputs are vectors of elements.

```assembly
# Signed dot-product
vfdot.vv vd, vs2, vs1, vm  # Vector-vector
```

```
# Dot product, SEW=32, EDIV=2
vfdot.vv vd, vs2, vs1, vm  # vd[i][31:0] += vs2[i][31:16] * vs1[i][31:16] + vs2[i][15:0] * vs1[i][15:0]

# Floating-point sub-vectors of two half-precision floats packed into 32-bit elements.
vsetvli t0, a0, e32,m1,d2  # Vectors of 32-bit elements, divided into 16b sub-elements
vfdot.vv v1, v2, v3  # v1[i][31:0] += v2[i][31:16]*v3[i][31:16] + v2[i][16:0]*v3[i][16:0]

# Floating-point sub-vectors of four half-precision floats packed into 64-bit elements.
vsetvli t0, a0, e64,m1,d4  # Vectors of 64-bit elements, divided into 16b sub-elements
vfdot.vv v1, v2, v3  # v1[i][31:0] += v2[i][31:16]*v3[i][31:16] + v2[i][16:0]*v3[i][16:0] +
                              # v2[i][63:48]*v3[i][63:48] + v2[i][47:32]*v3[i][47:32];
                              # v1[i][63:32] = -0 (NaN boxing)
```