University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2012

Topics for the Midterm Exam

The exam will be closed book/notes and cover material from week 1 through week 8. Problems will be in the style of homework problems, but in some cases more challenging and requiring synthesis of several concepts. A rough outline of important topics follows:

1. Introductory Material:
    - Concept of hierarchy in designs and example hierarchies.
    - Concept of cost/performance/power tradeoffs and simple examples.
2. Combinational Logic Basics:
    - Function of primitive logic gates.
    - Derivation of truth tables from simple combinational logic circuits.
    - Derivation of gate circuits from logic equations.
    - Derivation of canonical forms.
    - Algebraic manipulation for simplification and equivalence checking.
    - Signal restoration and its importance in digital circuits.
    - Operation and implementation of multiplexers.
3. FPGAs:
    - Idealized FPGA architecture model.
    - Details of basic FPGA PIP (programmable interconnection point).
    - LUT implementation details. Hierarchical LUT designs.
    - Partitioning logic circuits into LUTs and CLBs.
    - High-level details of Virtex 5 FPGAs (as presented in class).
4. Verilog HDL:
    - Concept of "behavioral" versus "structural" description.
    - Module specification and instantiation.
    - Basics of combinational logic and sequential circuit specification.
    - Continuous assignment versus procedural assignments (both blocking and non-blocking).
    - Specification of Finite State Machines.
    - Use of module parameters and "generate" constructs.

- Basic steps of logic synthesis and examples of how Verilog specifications are converted to circuits.
- Case versus nested If-else.
- Differences between HDL for synthesis and for simulation.
- Techniques for writing test-benches in Verilog.

5. State Elements and Sequential Circuits:

   - Basic flip-flop operation. Flip-flop Input/output/clock timing and constraints. Flip-flop reset types and functions.
   - "Register transfer" notion of sequential circuit timing. Waveform diagrams. Pipelining and signal feedback.
   - Level-sensitive latch operation. Implementation of flip-flops using level sensitive latches.
   - Flip-flop operation of Virtex 5 FPGA.

6. CPU microarchitecture:

   - Implementation of a single-cycle processor from ISA description.
   - Processor pipelining: impact on performance, hazard types and resolution.
   - Detailed operation of 3-stage MIPS pipeline.
   - Serial communication and UART basics.
   - Memory mapped CPU I/O and polling implementation.

7. Physical Design:

   - Chip-level design alternatives and pros and cons of each.
   - Economics of FPGAs versus ASICs.
   - CMOS circuits for basic logic gates, multiplexers, and flip-flops. CMOS transmission gates.
   - Implementation of tri-state buffers and their use for bidirectional communication.

8. Memory Blocks:

   - Naming conventions.
   - Internal organization.
   - SRAM Cell implementation.
   - Multiported memory internal organization.
   - Cascading memory blocks to increase width/depth/number of ports.
   - Virtex 5 block-RAM and LUT-RAM details and differences.
   - Operation and implementation of FIFO memories.
   - Principles behind DRAM operation.

9. Timing:

- Relation of clock speed to performance.
- Determination of maximum clock frequency from circuit.
- Origin of logic delay.
- Origin of flip-flop delay.
- Wire delay and mitigation.
- Effects of clock skew.
- Principle of flip-flop metastability. Clock synchronization.

10. Video:

    - Basics of Video display subsystem, with framebuffer and color map.
    - Decoupling CPU framebuffer writes from Video display.
    - Line drawing acceleration algorithm operation.