University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

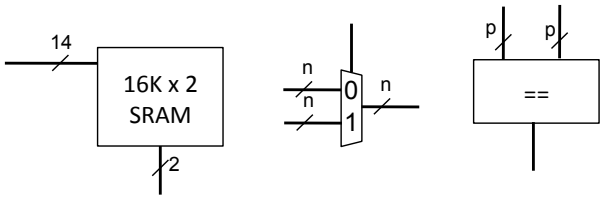
EECS150, Spring 2012

Homework Assignment 6: SRAM & DRAM
Due March 6^{th}, 2pm

1. A 64KB direct mapped cache is used in a system with 32 bit address space. Each cache line contains 4 bytes of data. How many bits are used to store the tags and data respectively? How about a 64KB 4 way associative cache with 8 bytes in each cache line?

2. For the Xilinx device we use in the lab (LX110T), what is the total amount of on-chip SRAM bits available to the user (not configuration bits)? Now counting BlockRAM only, what is the total memory read bandwidth, in bits/second? (Hint: maximum BlockRAM cycle rate is 400MHz.)

3. Assuming the we have a 32 bit address space, use the components shown in the diagram and a small number of two input gates to construct the datapath for a 128KB 4 way associative cache. Each cache line is 2 words and each word is 4 bytes. Your cache should include tag storage, data storage, address comparison, data output selection and any other parts you feel are relevant. You do not need to be concerned about the addressing of a byte within a word.



4. Assume we have a single banked DRAM where each row is 16 bytes and each individual request gets bursts of 4 bytes.

   (a) Assume we have no cache, what is the sequence of commands issued if the following loop is executed? Tabulate the addresses accessed, the targeted rows and the commands.

   (b) Now a direct-mapped cache is added, it has 4 byte cache lines and uses 4 indexing bits. What is the sequence of commands issued to the DRAM?

```
// assume A starts
// at addr 0x0
char A[56];
for(x1=0;x1<= 2;x1++)
{
  for (x2 = 2-x1 ; x2 <= 2 ; x2++)
  {
    for (x3 = x1; x3 <= x2 ; x3++)
    {
```

```
            A[7*x1+8*x2+9*x3]=  x3;
        }
    }
}
```

5. Assume you have a single bank DRAM in which each row is 32 bytes and each request gets burst of 8 bytes. How would you reorder the following memory accesses to minimize the time? What is the minimum number of requests the controller should buffer for this reordering to be possible?

   addresses to be accessed: 0x20, 0x32, 0x44, 0x30, 0x40, 0x52, 0x60

6. Given a DRAM with the same row size and burst size as in question 5, and you would be accessing the same sequence of addresses. Assuming you do not buffer/reorder the requests,

   (a) How would you bank the memory to minimize the time?

   (b) Which bits in the 32 bit address are you going to use for selecting the banks?