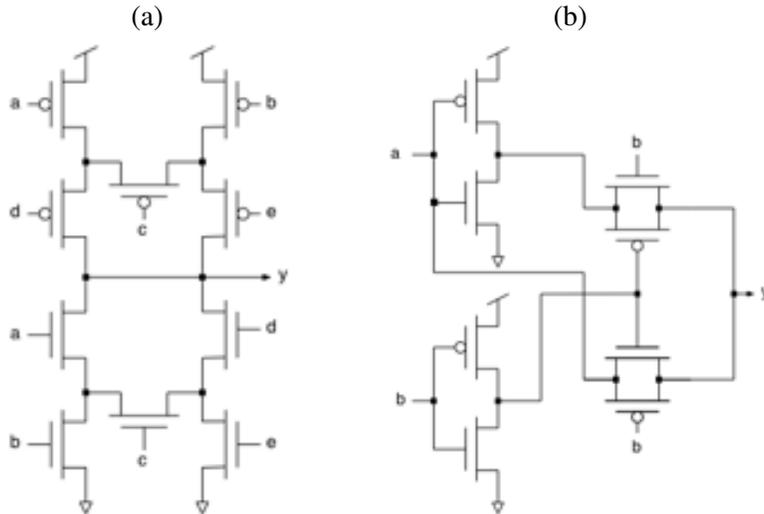


University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2012

Homework Assignment 5: CMOS Technology & SRAM
Due February 23th, 2pm

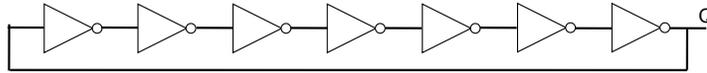
1. You have seen how a latch can be constructed using inverters and MOSFET, and how a D flip-flop can be constructed using two latches. Show modifications to the circuit to add the following. Try to minimize the total number of transistors:
 - (a) Synchronous reset
 - (b) Synchronous set
 - (c) Clock enable
 - (d) Asynchronous reset
2. For each of the CMOS circuits shown below, write a Boolean expression for the corresponding function?



3. Implement the following function using CMOS transistors, minimize the number of transistor you use. $f = (a + b)(c + d)$
4. Assume a product development based on an FPGA has a NRE cost of \$1M and a per unit FPGA cost of \$100. An ASIC version of the product has an NRE cost \$10M and a per unit cost of \$10. If your company is shipping 10,000 units, would you choose FPGA or ASIC? Why?
5. Using transmission gates, devise a circuit that implements the following 4-input function. Try to minimize the total number of transistors.

x_1x_0	y
00	0
01	a
10	b
11	1

6. A simple ring oscillator can be constructed from odd number of inverters (as shown). Suppose we use 7 inverters, each of which has a delay of 10ps,
- What would you expect to be the oscillation frequency?
 - How would you modify the circuit so that you could turn it on and off with a control signal?
 - How would you modify the circuit so that you could control the frequency (a few different frequency values is sufficient).



7. In this problem we will look at how a piece of the programmable interconnect portion of an FPGA might be implemented. Programming the connections generally happens at places where 4 signals/wires (north, south, east, west) meet. Using tri-state buffers, inverters, and/or transmission gates, show how you would implement a circuit that allows any one of the signals to drive any one or more of the other signals. Every signal should be buffered both on its way and on its way out - i.e., you can't just short the wires together, instead each signal must go through at least one tri-state or inverter. Try to minimize the number of transistors required for your implementation.
8. Consider the organization of a $256K \times 4$ -bit memory. Assume we desire a square array (same number of rows as columns)
- How many address bits total are required?
 - How many of the address bits are used for the row decoder?
 - How many of the address bits are used for the column muxing?

Now assume that we desire this memory to be “configurable”, in the sense that with some extra control we could use it as $512K \times 2$ -bit. Briefly describe what changes would need to be made to the memory block to allow the flexibility.

9. Suppose you are given a collection of configurable memory blocks. Each block can be configured as a $16K \times 1$, or a $8K \times 2$, ..., 512×32 . Your design problem requires a large memory that is $2K \times 32$. Which collection of smaller memory blocks would you choose and why? Show a block diagram of your design.