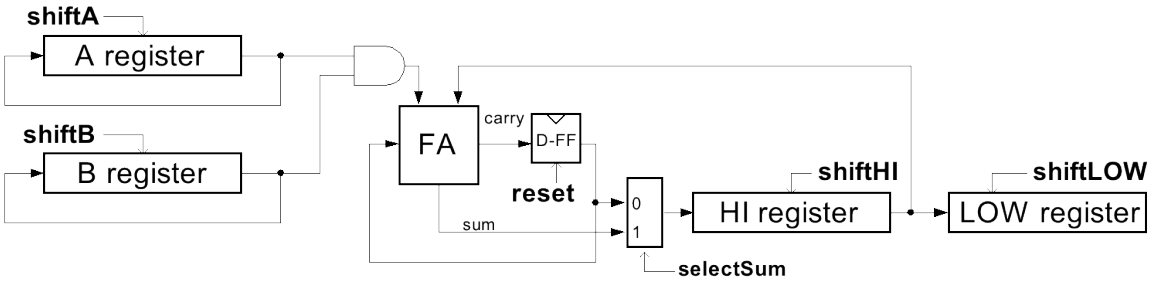
University of California at Berkeley
College of Engineering
Department of Electrical Engineering and Computer Science

EECS150, Spring 2012

Homework Assignment 10: Multiply, LFSR and High-level Design
Due April 12^{th}, 2pm

1. Shown below is a bit-serial multiplier.



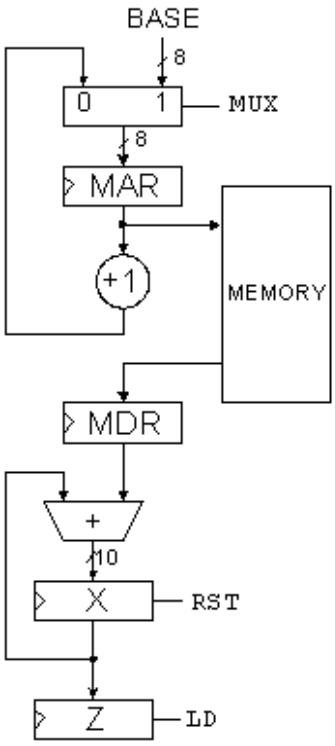
   (a) Tabulate the change of value in each register when 4'd6 is multiplied by 4'd10.

   (b) How should the multiplier be changed to handle signed 2's complement multiplication. Describe the change in the datapath, and rewrite the control algorithm you have seen in class.

2. Design an unsigned combinational multiplier (no flip-flops or controller) for multiplying the unsigned constant value 3900 by the variable X (X3X2X1X0). Using only full-adder cells and inverters, draw a circuit that implements the multiplier, minimizing the total amount of hardware and the delay from input to output. **Hint: think about carry-save addition.** What is the total number of FA cells used?

3. Design a circuit that can generate both 5 bit and 7 bit pseudo-random numbers. A control signal would switch the circuit between the 5-bit mode and 7-bit mode. When the circuit is used for generating 5 bit numbers, the top two bits of the output should remain low. Try to minimize the amount of hardware used.

4. A simple processor is designed to add the contents of blocks of 4 bytes in consecutive memory locations. The datapath is shown below



The processor has one data input (8-bit wide) named **BASE**, an input control signal named **ENABLE**, and 3 internal control signals - **MUX**,**LD**, and **RST**. The datapath contains three data registers - **MAR**, **MDR**, and **X**. After the processor performs its operation, the **Z** register is left with the sum of memory locations **BASE**, **BASE + 1**, **BASE + 2**, and **BASE + 3**. We assume that a controller (not shown) will take as input the **ENABLE** signal and generate **MUX**, **RST**, and **LD**. To begin the addition operation, an external circuit asserts **ENABLE** for 1 clock cycle then lowers it for a minimum of 12 cycles.

Write the register transfer language level description for the sequence of transfers that must occur after the **ENABLE** signal is asserted. Try to minimize the total number of cycles.