MOSFET Physical Parameters

OUTLINE

- Making Logic Gate Circuits
- Comparison of NMOS and CMOS
- Resistivity
- Resistance and Sheet Resistance

Reading

Mainly these presentation slides
Some Hambley 12.1-12.3

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Logic Gates – How are they built in practice?

A Valve is a Transistor \( V_{IN} \)

Current flows when \( V_{IN} \) is high Can be modeled by a 10k\( \Omega \) resistor

Valves in Series \( \Rightarrow \) NAND

Valves in Parallel \( \Rightarrow \) NOR

What goes in this box? How does it affect digital performance?

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Problems in the NMOS Inverter

Voltage Transfer Function: \( V_{OUT} \) vs. \( V_{IN} \)

The \( V_{OUT} \) vs. \( V_{IN} \) characteristic is another view of the logic gate that is used to determine the inverting and noninverting nature of a gate.

Voltage Transfer Function NMOS Inverter w/o Load

Complete a VTC like this for the device in the Homework
CMOS Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.

<table>
<thead>
<tr>
<th>VIN</th>
<th>Pull-Up Network</th>
<th>Pull-Down Network</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN-D</td>
<td>VOUT</td>
<td>VOUT</td>
</tr>
<tr>
<td>VIN-U</td>
<td>IOUT</td>
<td>IOUT</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VIN</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td></td>
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</tbody>
</table>

- p-type MOS Transistor (PMOS)
- n-type MOS Transistor (NMOS)

Find Points That Satisfies Both Devices for Each V_IN

<table>
<thead>
<tr>
<th>VOUT(V)</th>
<th>I_OUT(µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>100</td>
</tr>
<tr>
<td>3</td>
<td>60</td>
</tr>
<tr>
<td>5</td>
<td>20</td>
</tr>
</tbody>
</table>

Voltage Transfer Function for the CMOS Inverter Circuit

- Vertical section due to zero slope of I_OUT vs. V_OUT in the saturation region of both devices.

Current Density

The current density \( J \) is the current per unit area. If we have \( N \) positive charges per unit volume moving with average speed \( v \) in the +x direction, then the current density in the +x direction is just \( J = qNv \).

Example:
- \( v \) = 2 x 10^4 holes/cm^2 moving to the right at 2 x 10^4 cm/sec
- \( J = 1.6 x 10^{-19} x 2 x 10^{16} x 2 x 10^4 \) = 64 A/cm^2

Suppose this occurs in a conductor 2 \( \mu \)m wide and 1 \( \mu \)m thick:

\[ I = J \times A = 64 \times (2 \times 10^{-4} \times 1 \times 10^{-4}) = 1.28 \mu A \]

Electrical Conductivity \( \sigma \)

When an electric field is applied, current flows due to drift of mobile electrons and holes:

- electron current density: \( J_n = (-q)n \mu_n E \)
- hole current density: \( J_p = (+q)p \mu_p E \)
- total current density: \( J = J_n + J_p = (qn \mu_n + qp \mu_p)E \)

\[ \sigma \equiv qn \mu_n + qp \mu_p \] (Units: \( \Omega^{-1} \cdot \text{cm}^{-1} \))

Electrical Resistivity \( \rho \)

\[ \rho \equiv 1 \over \sigma = 1 \over qn \mu_n + qp \mu_p \]

- \( \rho \equiv 1 \over qn \mu_n \) for n-type mat'l
- \( \rho \equiv 1 \over qp \mu_p \) for p-type mat'l

(Units: ohm-cm)
Consider a Si sample doped with $10^{16}/\text{cm}^3$ Boron. What is its resistivity?

**Answer:**

\[ N_A = 10^{16}/\text{cm}^3, \quad N_D = 0 \quad (N_A >> N_D \rightarrow \text{p-type}) \]

\[ \rho = \frac{1}{q_n \mu_n + q_p \mu_p} \approx \frac{1}{q_p \mu_p} \]

\[ \approx \left(1.6 \times 10^{-19}\right)(10^{16})(450)^{-1} = 1.4 \Omega - \text{cm} \]

From $\mu$ vs. $(N_A + N_D)$ plot

**Example Calculation of Resistivity**

\[ \text{Example Calculation of Resistivity} \]

\[ \rho = \frac{L}{Wt} = \frac{R}{W} \Rightarrow R_s = \frac{\rho}{t} \]  
(Unit: ohms/square)

$L$, $W$, $t = \text{length, width, thickness}$  
$R_s$ is the resistance when $W = L$

- The $R_s$ value for a given layer in an IC technology is used
  - for design and layout of resistors
  - for estimating values of parasitic resistance in a circuit

\[ R = R_s, \quad R = R_s/2, \quad R = 2R_s, \quad R = 3R_s, \quad R \approx 2.6R_s \]

**Integrated-Circuit Resistors**

The resistivity $\rho$ and thickness $t$ are fixed for each layer in a given manufacturing process

A circuit designer specifies the length $L$ and width $W$, to achieve a desired resistance $R$

\[ R = R_s \frac{L}{W} \]  
(Unit: ohms/square)

**Example:** Suppose we want to design a 5 k$\Omega$ resistor using a layer of material with $R_s = 200 \Omega$.

**Resistance of Silicon Films (at low $E$ fields)**

at low fields \[ \sigma = q \frac{N}{\mu} \]  
where $N = n$ or $p$ and $\mu = \mu_n$ or $\mu_p$

So $\sigma = q n \mu_n$ for electrons in n-type Si  
and $\sigma = q p \mu_p$ for holes in p-type Si

In other words \[ R = 1/(q \mu_n N A) \] in N-type Silicon

Where $(N_A, t)$ is the number of donors implanted per unit area, and multiplying by $q$, we have the donor charge implanted per unit area. ($\mu_n$ is the mobility of the electrons).

Similarly \[ R = 1/(q \mu_p N A) \] in P-type Silicon

Where $(N_A, t)$ is the number of acceptors implanted per unit area, and multiplying by $q$, we have the acceptor charge implanted per unit area.

We do not need uniformly doping versus depth!

**Silicon Resistor by Ion Implantation**

**Example:** 1 $\mu$m thick n-type silicon layer which was implanted with $10^{11}$ donors cm$^{-2}$. (Thus $N_d = 10^{12} / 10^4 = 10^8$ cm$^{-2}$)

$\sigma = q n \mu_n = (1.6 \times 10^{-19} \text{C})(10^{18} \text{cm}^{-3})(1000 \text{cm}^2 / \text{Vsec}) = 1.6 \text{S/cm}$

$\rho = 1/\sigma = 0.625 \Omega \text{cm}$

Sheet resistivity, $R$ given by:

\[ R = \frac{1}{2 \rho} = 6.25 \text{ K}\Omega /\text{square} \]

But this can be obtained directly from the implant "Q" of $1.6 \times 10^{10} / 10^4 = 1.6 \times 10^6$ thus

\[ R = \frac{1}{2 \rho Q} = 6.25 \text{ K}\Omega /\text{square} \]

**Physics of Current Flow, Resistance, Resistivity**

\[ E = \frac{V}{L} \]

\[ I = \frac{V}{R} \]

$L$, $W$, $t = \text{length, width, thickness}$

\[ R = \frac{\rho L}{A} = \frac{1}{q \mu N} \frac{L}{W t} \]

From $\mu$ vs. $(N_A + N_D)$ plot

\[ q N t \] has the dimensions of charge per unit area and represents the charge per unit area in a film of thickness $t$ when the film has $N$ carriers/cm$^3$ and is $t$ units thick. Thus we call $q N t$ the "Q" and $R = (L/W)/M = L/W R_s$.

Where $R_s$ is the resistance of a "square" of the film. Clearly if $L$ is four times $W$, then $R = 4 R_s$.

**Sheet Resistance $R_s$**

\[ R = \frac{L}{Wt} = \frac{R_s}{W} \quad \Rightarrow \quad R_s = \frac{\rho}{t} \]  
(Unit: ohms/square)

$R_s$ is the resistance when $W = L$

- The $R_s$ value for a given layer in an IC technology is used
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**Resistor layout (top view)**

**Space-efficient layout**
Device Layout and Process

Process Flow
- Active Area
- n-Well Implant
- Poly
- n Source/Drain
- p Source/Drain
- Insulator
- Contacts
- Metal

Device Layout Compensates Mobility Diff.

- The desired device current drive can be changed by adjusting the device layout.
- A lower mobility PMOS pull-up device can be made larger than the associated NMOS pull-down device for better balance.