MOSFET Physical Parameters

Lecture 29, 11/07/05

OUTLINE

- Making Logic Gate Circuits
- Comparison of NMOS and CMOS
- Resistivity
- Resistance and Sheet Resistance

Reading

Mainly these presentation slides
Some Hambley 12.1-12.3

Midterm #2 Exam Results
Logic Gates – How are they built in practice?

A Valve is a Transistor $V_{IN}$

- Current flows when $V_{IN}$ is high
- Can be modeled by a $10k\Omega$ resistor

Valves in Series $\Rightarrow$ NAND

Valves in Parallel $\Rightarrow$ NOR

What goes in this box?

How does it affect digital performance?

Voltage Transfer Function: $V_{OUT}$ vs. $V_{IN}$

The $V_{OUT}$ vs. $V_{IN}$ characteristic is another view of the logic gate that is used to determine the inverting and noninverting nature of a gate.
Problems in the NMOS Inverter

Problem #1
Current when $V_{OUT}$ Low

Problem #2
Poor $V_{OUT}$ High with Load

Open Load

Load

Voltage Transfer Function NMOS Inverter w/wo Load

Complete a VTC like this for the device in the Homework
CMOS Inverter Example

It may be simpler to just think of PMOS and NMOS transistors instead of a general 3 terminal pull-up or pull-down devices or networks.

Find Points That Satisfies Both Devices for Each $V_{IN}$

![Graph showing solution points for different $V_{IN}$ values](image-url)
Voltage Transfer Function for the CMOS Inverter Circuit

Current Density

The current density \( J \) is the current per unit area
\( (J = \frac{I}{A}; A \) is the cross-sectional area of the conductor)

If we have \( N \) positive charges per unit volume moving with average speed \( v \) in the \(+x\) direction, then the current density in the \(+x\) direction is just \( J = qNv \)

Example:
- \( N = 2 \times 10^{16} \) holes/cm\(^3\) moving to the right at 2 x 10\(^4\) cm/sec
- \( J = 1.6 \times 10^{-19} \times 2 \times 10^{16} \times 2 \times 10^4 = 64 \text{ A/cm}^2 \)

Suppose this occurs in a conductor 2 \( \mu \text{m} \) wide and 1 \( \mu \text{m} \) thick:
\[
I = J \times A = 64 \times (2 \times 10^{-4} \times 1 \times 10^{-4}) = 1.28 \mu\text{A}
\]
**Electrical Conductivity $\sigma$**

When an electric field is applied, current flows due to drift of mobile electrons and holes:

- **Electron current density:** $J_n = (-q)nv_n = qn\mu_n E$

- **Hole current density:** $J_p = (+q)pv_p = qp\mu_p E$

- **Total current density:** $J = J_n + J_p = (qn\mu_n + qp\mu_p)E$

$$J = \sigma E$$

**Conductivity**

$$\sigma \equiv qn\mu_n + qp\mu_p$$  (Units: $\Omega$-cm$^{-1}$)

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**Electrical Resistivity $\rho$**

$$\rho \equiv \frac{1}{\sigma} = \frac{1}{qn\mu_n + qp\mu_p}$$

- $\rho \approx \frac{1}{qn\mu_n}$ for n-type mat'l

- $\rho \approx \frac{1}{qp\mu_p}$ for p-type mat'l

(Units: ohm-cm)
Consider a Si sample doped with $10^{16}$/cm$^3$ Boron. What is its resistivity?

**Answer:**

$N_A = 10^{16}$/cm$^3$, $N_D = 0$ \hspace{1cm} ($N_A >> N_D \rightarrow p$-type)

$\rightarrow p \approx 10^{16}$/cm$^3$ and $n \approx 10^4$/cm$^3$

$$\rho = \frac{1}{qn\mu_n + qp\mu_p} \approx \frac{1}{qp\mu_p}$$

$$= \left[ (1.6 \times 10^{-19}) (10^{16}) (450) \right]^{-1} = 1.4 \ \Omega - \text{cm}$$

*From $\mu$ vs. $(N_A + N_D)$ plot*

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**Example Calculation of Resistivity**

**Physics of Current Flow, Resistance, Resistivity**

$$E = \frac{V}{L}.$$  

$$I = \frac{V}{R}.$$  

$$R = \rho \frac{L}{A} = \frac{1}{qN}\frac{L}{W} t = \frac{(L/W)}{\mu(qN)}.$$ 

But $qN t$ has the dimensions of charge per unit area and represents the charge per unit area in a film of thickness $t$ when the film has $N$ carriers/cm$^3$ and is $t$ units thick. Thus we call $qN t$ the "Q" and

$$R = \frac{(L/W)}{\mu Q} = \frac{L}{W} R.$$  

Where $R$ is the resistance of a "square" of the film. Clearly if $L$ is four times $W$, then $R = 4 R$. 

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Sheet Resistance $R_s$

\[
R = \rho \frac{L}{Wt} = R_s \frac{L}{W} \quad \Rightarrow \quad R_s = \frac{\rho}{t} \quad \text{(Unit: ohms/square)}
\]

(L, W, t = length, width, thickness)  

- $R_s$ is the resistance when $W = L$

- The $R_s$ value for a given layer in an IC technology is used
  - for design and layout of resistors
  - for estimating values of parasitic resistance in a circuit

\[
\begin{align*}
R &= R_s \\
R &= R_s/2 \\
R &= 2R_s \\
R &= 3R_s
\end{align*}
\]

Integrated-Circuit Resistors

The resistivity $\rho$ and thickness $t$ are fixed for each layer in a given manufacturing process

A circuit designer specifies the length $L$ and width $W$, to achieve a desired resistance $R$

\[
R = R_s \left( \frac{L}{W} \right)
\]

**Example:** Suppose we want to design a 5 kΩ resistor using a layer of material with $R_s = 200 \ \Omega/\square$

Resistor layout (top view)  
Space-efficient layout
Resistance of Silicon Films (at low \( E \) fields)

at low fields \( \sigma = q \ N \ \mu \) where \( N = n \) or \( p \) and \( \mu = \mu_n \) or \( \mu_p \)

So \( \sigma = q \ n \ \mu_n \) for electrons in n-type Si
and \( \sigma = q \ p \ \mu_p \) for holes in p-type Si

In other words \( R = 1/ \mu N (qN_d t) = 1/ \mu N (Q_d) \) in N-type Silicon

Where \((N_d, t)\) is the number of donors implanted per unit area,
and multiplying by \( q \), we have the donor charge implanted per unit area. (\( \mu_n \) is the mobility of the electrons).

Similarly \( R = 1/ \mu p (qN_A t) = 1/ \mu p (Q_A) \) in P-type Silicon

Where \((N_A, t)\) is the number of acceptors implanted per unit area, and multiplying by \( q \), we have the acceptor charge implanted per unit area.

We do not need uniformly doping versus depth!

Silicon Resistor by Ion Implantation

Example: 1 \( \mu \)m thick n-type silicon layer which was implanted with \( 10^{12} \) donors cm\(^{-2} \). (Thus \( N_d = 10^{12} / 10^{-4} = 10^{16} \) cm\(^{-3} \) )
\(
\sigma = q \ n \ \mu_n = (1.6 \times 10^{-19} \) C \( ) (10^{16} \) cm\(^{-3} \) \( ) (1000 \) cm\(^2\) / Vsec \( ) = 1.6 \) S/cm
\( \rho = 1 / \sigma = 0.625 \) \( \Omega \) cm

Sheet resistivity, \( R \) given by:
\( R = [1/(\sigma \ t)] = 6.25 \) K \( \Omega \) /square

But this can be obtained directly from the implant
"\( Q \)" of \( 1.6 \times 10^{-19} \times 10^{12} = 1.6 \times 10^{-2} \) thus
\( R = [1/(Q \ \mu)] = 6.25 \) K \( \Omega \) /square

\[ R_{AB} = 4 \times 6.25 = 25 \) K\( \Omega \]
Device Layout and Process

Process Flow
- Active Area
- n-Well Implant
- Poly
- n Source/Drain
- p Source/Drain
- Insulator
- Contacts
- Metal

Device Layout Compensates Mobility Diff.

- The desired device current drive can be changed by adjusting the device layout.
- A lower mobility PMOS pull-up device can be made larger than the associated NMOS pull-down device for better balance.