PROBLEM SET #3

Issued: Tuesday, Sep. 17, 2014
Due: Wednesday, Sep. 24, 2014, 8:00 a.m. in the EE 143 homework box near 140 Cory

• Layout to Cross-Section

1. Consider the following layout of an integrated circuit and the corresponding process flow:

The Process Flow

1) Silicon oxidation: target = 300nm
2) Lithography: Mask I (N-well)
3) Etch SiO₂
4) Remove PR
5) N-well diffusion: P (n-type)
6) Etch SiO₂
7) Silicon oxidation: target = 100nm
8) LPCVD Si₃N₄: target = 500nm
9) Lithography: Mask II (Active)
10) Etch Si₃N₄
11) Etch SiO₂
12) Field isolation implant: B+ (p-type)
13) Remove PR
14) Grow 1μm of SiO₂ thermally (LOCOS oxidation)
15) Etch Si₃N₄
16) Etch SiO₂
17) Dry oxidation for gate oxide:
   target = 100nm
18) Lithography: Mask III (Buried Contact)(dark field)
19) Etch SiO₂
20) Remove PR
21) LPCVD in situ phosphorous-doped gate polysilicon: target = 350nm
22) Lithography: Mask IV (Poly)
23) Dry etch polysilicon
24) Remove PR
25) Lithography: Mask V (n+ implant)(dark field)
26) D/S ion implantation: P (n-type)
27) Remove PR
28) Lithography: Mask VI (p+ implant)(clear field)
29) D/S ion implantation: B (p-type)
30) Remove PR
31) Anneal at 1050°C to activate dopants and drive-in diffusion
32) LPCVD PSG: target = 1 μm and reflow at 950°C
33) Lithography: Mask VII (Contact)
34) Etch SiO₂ down to S/D regions and polysilicon
35) Remove PR
36) Deposit Al: sputtering target = 1 μm
37) Lithography: Mask VIII (Metal)
38) Dry etch Al
39) Remove PR

(a) Suppose positive photoresist is used in all lithography steps. What is the polarity (i.e., dark or clear field) for Mask I and II, Mask IV, and Mask VII and VIII?

(b) Plot the cross-sections along AA’ and BB’ planes, through step 14), 20), and 39).

2. Suppose that the following process flow is used to achieve a MEMS cantilever as shown below together with its cross-section along AA’ plane. Note that the cantilever is similar to that in HW#2 Problem 2 but now with an additional bottom electrode layer for electrical access.

**MEMS Cantilever Process Flow**

1) Start with a Si wafer
2) LPCVD Si₃N₄: target = 500nm
3) LPCVD in situ phosphorous-doped polysilicon: target = 300nm
4) Lithography: Mask I (Bottom Electrode)
5) Dry etch polysilicon
6) Remove PR
7) LPCVD SiO₂: target = 300nm
8) Lithography: Mask II (Anchor)
9) Etch SiO₂
10) Remove PR
11) LPCVD in situ phosphorous-doped polysilicon: target = λ
12) Lithography: Mask III (Beam)
13) Dry etch polysilicon
14) Remove PR
15) Release in liquid HF
(a) How high does the cantilever suspend from the bottom electrode (i.e., dimension of $d$)?

(b) Assume $\lambda = 5 \, \mu m$. Draw a layout for the cantilever on graph paper (which is provided) with each box corresponding to one $\lambda$ (i.e., 5 $\mu m$). Label dimensions whenever they are applicable and indicate each of the mask layers (i.e., Mask I (Bottom electrode), Mask II (Anchor) … etc.).