EE143 LAB

W/L = 15/4 μm

MOSFET 9a (PART A)

ID (A)

VD (V)

-2.0E-05 0.0E+00 2.0E-05 4.0E-05 6.0E-05 8.0E-05 1.0E-04 1.2E-04 1.4E-04 1.6E-04 1.8E-04

VG = 0V
VG = 1V
VG = 2V
VG = 3V
VG = 4V
VG = 5V
VG = 6V
VG = 7V
Guidelines for Process Integration

* A sequence of **Additive** and **Subtractive** steps with **lateral patterning**

- Watch out for materials compatibility issues (e.g. temperature limit)
- Planarity is desirable for lithography, etching, and thin-film deposition
- Whenever possible, use self-aligned structures
Processing Temperature and Material Failure Temperature

Si Melting Point (1412°C)

Al-Si Eutectic (560°C)
Self-Aligned Silicide Process (SALICIDE) using Ion Implantation and Metal-Si reaction

*Process Flow: Show Process Description and Cross-sections
A Generic CMOS Process

P-well CMOS
Layout Design Rules

• Understand the meaning of the boundaries

• Use EE143 design rule values

• Actual layout may look different from conceptual layout when rule values are applied

• Change of design rules values will need understanding of device structures/technology
  • (qualitative)

“conceptual layout”
Summary: Parameters Affecting $V_T$

1. $\phi_M$
2. $x_{ox}$
3. $N_a$
4. $V_B$
5. $V_C$
6. $\rho_{OX}$ & $Q_f$
7. Dopant implant near Si/SiO$_2$ interface

$V_G - V_B = \Phi_{MS} + V_{ox} + V_{Si}$
Voltage drop = area under E-field curve

Accumulation

\[ V_{ox} = \frac{Q_a}{C_{ox}} \]
\[ V_{Si} \approx 0 \]

Depletion

\[ V_{ox} = qN_a x_d / C_{ox} \]
\[ V_{Si} = qN_a x_d^2 / (2 \varepsilon_s) \]

Inversion

\[ V_{ox} = \left[ qN_a x_{d_{max}} + Q_n \right] / C_{ox} \]
\[ V_{Si} = qN_a x_{d_{max}}^2 / (2 \varepsilon_s) = 2 |\Phi_F| \]

* For simplicity, dielectric constants assumed to be same for oxide and Si in E-field sketches
$+Q_f$ or $Q_{ox}$

$n^+$ polysilicon gate

$X_{ox} = 50$ nm

$Q_{tot} = 0$

$X_{ox}$ increases

$|V_{CB}|$ increases

$\Phi_M$ decreases

$|V_{CB}|$ increases

$\Phi_M$ increases

$X_{ox}$ increases

$X_{ox}$ increases

$V_{CB}$ increases

Substrate concentration, $N_B$ (atoms/cm$^3$)
MOSFET I-V Characteristics

For $V_D < V_{Dsat}$

$$I_D = \frac{\mu_n W}{L} C_{OX} \left( V_G - V_T - \frac{V_{DS}}{2} \right) V_{DS}$$

For $V_D > V_{Dsat}$

$$I_D = I_{Dsat} = \frac{\mu_n W}{2L} C_{OX} (V_G - V_T)^2$$

Note: $V_{Dsat} = V_G - V_T$
Small Signal Capacitance $C$ ($\equiv \Delta Q/\Delta V_G$)

$C_{ox}$

$p$-type substrate

**Table:**

<table>
<thead>
<tr>
<th>Voltage limits</th>
<th>$V' &lt; 0$</th>
<th>$V' &gt; 0$</th>
<th>$\phi_{d, Si} \geq 2\phi_F$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Charge storage</td>
<td>Majority carriers</td>
<td>Dopant ions in depletion layer</td>
<td>Minority carriers</td>
</tr>
</tbody>
</table>
| Capacitance   | $C_o = \frac{\varepsilon_{ox}}{x_o}$ | $C = \left(\frac{1}{C_o} + \frac{1}{\varepsilon_s / x_d}\right)^{-1}$ | Low frequency: $C_o$
High frequency: $\left(\frac{1}{C_o} + \frac{1}{\varepsilon_s / x_{d, max}}\right)^{-1}$ |
Typical Thin Film stress: $10^8$ to $5 \times 10^{10}$ dynes/cm$^2$ ($10^7$ dyn/cm$^2$ = 1 MPa)

Radius of Curvature of warpage

$$r = \frac{E_s \times t_s^2}{(1 - v)_s \times 6 \times \sigma_f \times t_f}$$

“Stoney Equation”
MEMS Process Flow Example:

to form a hollow cantilever beam
MEMS- IC Integration

Example of MEMS-first approach
Thermal Oxidation Model

Note: $C_s \neq C_o$

- $C_G$:
  - stagnant layer

- $C_s$:

- $C_o$:

- $C_i$:

- $X_{0x}$:

- $F_1$:
  - gas transport flux

- $F_2$:
  - diffusion flux through SiO$_2$

- $F_3$:
  - reaction flux at interface
CVD Deposition Rate [Grove Model]

\[
\frac{D}{\delta} = h_G
\]

\[
k_s = k_o e^{-\Delta E / kT}
\]

\[
F_1 = \frac{D [ C_G - C_S]}{\delta}
\]

\[
F_3 = k_s C_S
\]

\[
F_1 = F_3
\]

\(\delta\) = thickness of stagnant layer
Ion Implantation

\[ C(x) = C_p \cdot e^{-\frac{(x-R_p)^2}{2(\Delta R_p)^2}} \]

- \( R_p = \text{projected range} \)
- \( \Delta R_p = \text{longitudinal straggle} \)

Implantation Damage

Ion Channeling

Si Crystal

deeper penetration

random scattering path
Examples: Well drive-in and S/D annealing steps

Thermal Budget

\[(Dt)_{\text{effective}} = \sum_i (Dt)_i\]

For a complete process flow, only those steps with high Dt values are important.
Projection Printing Considerations

(1) Resolution

\[ l_m = k_1 \frac{\lambda}{NA} \]

\[
\begin{bmatrix}
0.6 \frac{\lambda}{NA} \\
\text{typical}
\end{bmatrix}
\]

\[ NA \equiv \text{numerical aperture of lens} . \]

= \sin \theta

\[ k_1 = \text{a constant between 0.25 and 1, depending on optics, resist, and process latitude} \]
Depth of Focus (DOF)

\[ \Delta z = k_2 \frac{\lambda}{(NA)^2} \]

\[ 0.5 < k_2 < 1 \]

\[ \Delta z \approx \pm \frac{l_m}{2 \tan \theta} \approx \pm \frac{l_m}{2 \sin \theta} = \pm \frac{\lambda}{2(NA)^2} \]

for small \( \theta \)
Past Exam Question

Answer
Worst-Case Design Considerations for Etching

- Step height variation
- Variation of film thickness across wafer
- Etching mask can be eroded during film etching

Substrate

Mask
Effect of RIE process variables on etching characteristics
Multilevel Metallization

Interconnect

Via
Electromigration Issues

Fig. 5 Cross-sectional TEM micrographs of the TiN/Al-Si-Cu/ 
TiN/Al-Si-Cu/TiN/Ti interconnection.

Grain boundaries on films do not overlap 
Hence voids in the two metal layers do not overlap 
The TiN between the two layers prevents voids 
from propagating between the layers.

"A quarter micron interconnection technology using Al-Si-Cu/TiN layers" 
T.Kikkawa et al, IEDM 91 pg 281