Importance of Layer-to-Layer Alignment

Example: metal line to contact hole

→ marginal contact

→ no contact!

Example of Design Rule:
If the minimum feature size is $2\lambda$, then the safety margin for overlay error is $\lambda$.

→ Design Rules are needed:
- Interface between designer & process engineer
- Guidelines for designing masks
IC RESISTOR MASK LAYOUTS – REGISTRATION OF EACH MASK

Registration of mask patterns is critical → show separate layouts to avoid ambiguity

Registration of one mask to the next (also called “alignment” and “overlay”) is a crucial aspect of lithography
Same Layout but with misregistration (misalignment)

perfect registration

A

B

scale in \( \mu m \)
for B-B “cut”

2 \( \mu m \)

Contact mask misaligned by 2 \( \mu m \)

A

B

scale in \( \mu m \)
for B-B “cut”

Lets look again at cross-section A-A to understand the consequence of this misalignment. Note contact mask 2 \( \mu m \)
Layout with no misregistration (misalignment)

perfect registration

STEP 7

p-type layer

Al
Thus we need safety margins in layout which take into account the possible tolerances in fabrication. Each process has a set of "design rules" which specify the safety margins.
(1) Absolute-Value Design Rules
   * Use absolute distances

(2) $\lambda$ -based Design Rules
EE143 Layout Design Rules

1. Basic length unit = $\lambda = 2\mu$m

1.1 Lithography and etching limit $= 2\lambda$

1.2 Overlay accuracy $= \lambda$
2.1 Metal-Si Contact Hole

(same rule for Metal-poly)

Min. contact hole = $2\lambda \times 2\lambda$

Min contact hole to diffusion layer distance = $\lambda$
2.2. Metal Lines

Min width = $2\lambda$

Min. metal-metal spacing = $3\lambda$

[Rationale] metal runs on rough topography

$3\lambda$ spacing to ensure no shorting between the 2 lines.
Min overlap of contact hole  = $\lambda$

Etching problem

CVD SiO$_2$ deposition. problem in narrow gap
Metal line-width is larger when running over a contact hole

Configuration 1

Configuration 2
2.3 Poly-Si Lines

Min width = $2\lambda$

Min poly-poly spacing = $2\lambda$

[Rationale: Unlike metal lines, poly-Si runs on smoother topography]

Min underlap of metal/poly contact = $\lambda$

$4\lambda \times 4\lambda$
Example: Metal Contact to Poly

Note: Both metal and poly linewidths will enlarge to accommodate contact hole overlay error $\lambda$. 
2.4. MOS Thin-Oxide Region

Min Width = $2\lambda$

Min spacing = $3\lambda$

Thick Oxide Region (FOX)

Thin Oxide Region (active device area)
Min underlap of thin-oxide contact $= \lambda$
3. Poly-Si Gate

Min gate-overlap of field oxide = $2\lambda$

[Comment] Avoid n+ channel formation during S/D Implant

ideal

With overlay error
Min thin-oxide contact to gate spacing = 2 $\lambda$
Comment:
Al to poly contact should not be directly on top of gate oxide area

Gate oxide

Si

Poly gate

Al

Poly

SiO₂

Si

~400°C

Al spike

Poly

SiO₂

Si
Al contact on thick oxide area ok

$2\lambda$

SiO$_2$ (CVD)

FOX
Min Gate Width = \(2 \lambda\)

Min Gate Length = \(2 \lambda\)

Usually: W/L are specified by circuit requirement.

Min. poly to thin oxide spacing = \(\lambda\)
Example: Design a minimum-size poly-gate MOS transistor with $W/L = 4\mu m/4\mu m$ ($2\lambda \times 2\lambda$)

Minimum size contact = $2\lambda \times 2\lambda$
Minimum thin-oxide-region underlap of contact = $\lambda$
Minimum source/drain contact to gate spacing = $2\lambda$
Minimum $L = 2\lambda$, Minimum $W = 2\lambda$
Minimum gate overlap of field-oxide region = $2\lambda$
Minimum metal overlap of contact = $\lambda$
Minimum thin-oxide-region to thin-oxide-region spacing = $3\lambda$
* Layout area /transistor = $15\lambda \times 7\lambda = 105 \lambda^2$