CMOS Inverter Layout

Note body contacts:
- p-well to GND
- n-substrate to $V_{DD}$

- P-well mask (dark field)
- Active (clear field)
- Gate (clear field)
- Select mask (dark field & clear field)
- Contact (dark field)
- Metal (clear field)
Visualizing Layouts and Cross-Sections with SIMPLer

SIMPL is a CAD tool created by Prof. Neureuther’s group

- allows IC designers to visualize device cross-sections corresponding to a fabrication process and physical layout.

A Berkeley undergraduate student, Harlan Hile, created a mini-version of SIMPL (called SIMPLer) for EE40.

- It’s a JAVA program -> can be run on any computer, as well as on a web server.

- A 3D version SIMPL-GL can be accessed at http://cuervo2.eecs.berkeley.edu/Volcano/simpl_gl/main.htm
Step Number 3

- Implant donors with a concentration of $10^4$ ions per cm² and anneal to a depth of 2500 nanometers.
Step Number 12

implant acceptors

with a concentration of $10^{12}$ ions per cm$^2$ and anneal to a depth of 500 nanometers.

Materials Key

- N-type Si
- Neutral Si
- P-type Si
- Oxide
- Polysilicon
- Metal

Width:Height ratio is ~1.2
Step Number 15

implant donors

with a concentration of 10^12 ions per cm^2

and anneal to a depth of 500 nanometers.
Step Number 17

pattern oxide

with a dark field mask. Use the color magenta and the pattern solid to display this mask. The current draw mode is:

- draw
- erase

Mask Key

- Step 2, oxide dark field
- Step 4, oxide clear field
- Step 6, oxide dark field
- Step 9, poly clear field
- Step 11, photo dark field
- Step 14, photo clear field
- Step 17, oxide dark field

Materials Key

- N-type Si
- Neutral Si
- P-type Si
- Oxide
- Polysilicon
- Metal

Width:Height ratio is ~1.2
Step Number 19

Pattern metal

With a **clear** field mask. Use the color **cyan** and the pattern **X's** to display this mask. The current draw mode is:

- **draw**
- **erase**

Delete Step  Add Step
 Restart  Calculate Cross-Section

Materials Key

- **N-type Si**
- **Neutral Si**
- **P-type Si**
- **Oxide**
- **Polysilicon**
- **Metal**

Width:Height ratio is ~1.2

Mask Key

- Step 2, oxide dark field
- Step 4, oxide clear field
- Step 6, oxide dark field
- Step 9, poly clear field
- Step 11, photo dark field
- Step 14, photo clear field
- Step 17, oxide dark field
- Step 19, metal clear field

Professor N Cheung, U.C. Berkeley
Twin Well + STI CMOS Process

1. Define active areas; etch Si trenches
   Fill trenches (deposit SiO₂ then CMP)

2. Form wells (implantation + thermal anneal)

3. Grow gate oxide
   Deposit poly-Si and pattern gate electrodes

4. Implant source/drain and body-contact regions
   Activate dopants (thermal anneal)

5. Deposit insulating layer (SiO₂); planarize (CMP)
   Open contact holes; deposit & pattern metal layer
3D view of a CMOS inverter after contact etch.
Well Engineering

P-tub

N-tub

Twin Tub

Various CMOS structures. (a) p tub. (b) n tub. (c) twin tub.
Twin Well CMOS Process Flow

(a) Si$_3$N$_4$ deposition
(b) P-well implantation
(c) Boron implantation
(d) n-well implantation
(e) Metal deposition
Retrograde Well

- formed by high energy (>200keV) implantation

Conventional well (depth and profile controlled by diffusion drive-in)

Retrograde well (depth and profile controlled by implantation energy and dose)
1) Very low thermal budget for well formation (no need for diffusion drive-in)

2) Retrograde Well is formed AFTER field oxidation ⇒ small lateral diffusion and localized high conc under FOX
Example: Formation of Channel Stop and Retrograde Well in a single step

Channel stop

Retrograde well
Multiple Implants for Well Engineering

Advanced “Profiled” Wells for Sub-Micron Devices
(after Reference 136)

A. N-Well Vertical Profile* (under the gate)

- $10^{19}$
- $10^{18}$
- $10^{17}$
- $10^{16}$
- $10^{15}$

CONCENTRATION (cm$^{-3}$)

0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 1.1 1.2 1.3

DEPTH (µm)

- Vth CONTROL
- BURIED CHANNEL DEPTH CONTROL
- S/D JUNCTION CAPACITANCE
- HOT CARRIER CONTROL
- PUNCHTHROUGH SUPPRESSION
- CHANNEL STOP

- LATCH-UP SUPPRESSION
- SOFT ERROR REDUCTION

PHOSPHORUS: 600keV, 3x10$^{13}$ cm$^{-2}$

PHOSPHORUS: 70keV, 6x10$^{12}$ cm$^{-2}$

PHOSPHORUS: 200keV, 4x10$^{12}$ cm$^{-2}$

NET DOPING PROFILE

AS IMPLANTED
Channel Engineering

SUBMICRON DEVICE STRUCTURE AND DESIGN

Vertical (Channel) Engineering

Horizontal (Drain) Engineering

Spacer Formation Technology

Polysilicon Gate Stack Design

Shallow Oxide Trench Isolation

Low Series Resistance Contact Technology

Deep S/D and LDD Tab Design

Channel Profile Design

LDD Profile Design

Drain Profile Design
Generic Silicon-on-Insulator (SOI) CMOS Process Flow

(a) 

(b) 

(c) 

(d) 

(e)
SOI Process Flow (continued)
Self-Aligned Channel V-gate by Optical Lithography (SALVO) Process

- Smallest feature printable by lithography
- Oxide spacer
- poly-Si gate
- Normal S/D implant
- CVD oxide
- SiO$_2$
- TiSi$_2$
- Angled Implant
- n+ pocket
- Thermal gate oxide
- * Sub-50nm channels
SALVO Process Flow

See Homework Problem

Chang et al, IEDM 2000
SUMMARY OF IC PROCESS INTEGRATION MODULE

• Self aligned techniques: channel stop, Source/Drain, LDD, SALICIDE
• How to read process flow descriptions and cross-sections
• Generic NMOS Process with LOCOS
• Generic CMOS Process with LOCOS and single well
• Modified Processes:
  • Shallow Trench Isolation (STI), Twin Wells, Retrograde Well, SOI CMOS