Sample Solutions

Instructions: DO ALL WORK ON EXAM PAGES

Make sure your copy of the exam paper has 11 pages (including cover page)
This is a 3-hr exam (12 sheets of handwritten notes allowed)

Grading: Whenever possible, use sketches to support your explanation.
Show correct units and algebraic sign for numerical answers.
No partial credit for numerical answers orders of magnitude off.

Problem 1 (40 points)

Problem 2 (20 points)

Problem 3 (40 points)

Problem 4 (40 points)

Problem 5 (35 points)

Problem 6 (25 points)

TOTAL (200 points)
Problem 1 Lab Questions (40 points total)

(a) (10 points) In Cory 218, we only have the following processing equipment:
- Mask aligner
- Spinning, baking, and development setups for photoresist and spin-on glass
- Wet chemical bench for cleaning and wet etching
- Oxidation furnace
- Annealing furnace
- Al evaporator.

Describe a process sequence using ONLY the available equipment in Cory 218 to fabricate the following DRAM structure, which is simply an Al-gate n-channel MOSFET connected to a capacitor:

1) Spin on phosphorus doped SOG.: n+ region patterning (Mask 1). Drive-in.
2) Strip SOG. Thermal oxidation to form field oxide.
3) Gate oxide patterning after field oxide growth (Mask 2). Grow thin gate oxide.
4) Contact opening (Mask 3)
5) Aluminun deposition.: Metal patterning (Mask 4)
Problem 1 Lab Questions continued
(b) (8 points) Suppose the lab has an ion implanter, which step(s) in the process sequence will you change to improve the MOS device performance of the Ee143 chip? What improvement will you expect?

Replace all SOG doping of poly-Si and source/drain by ion implantation. More precise control of dose and junction depths. The shortest channel device will work because of less lateral diffusion.

Can also perform threshold implant to control $V_T$ if desired.

(c)(4 points) The ring oscillator test structure on the EE143 chip usually has low yield. What are the major problems?

ALL components of the oscillator (transistors, contacts, and interconnects) have to work. If anyone of the components fails, the oscillator will not function.

Most common problems: misalignment, overetch, contact cleaning.

(d) (4 points) Why do we anneal the chip with forming gas after metallization?

1) Reduce interface charge of the Si/SiO2 interface by hydrogen passivation
2) Enhance Al diffusion through oxide residual left by surface cleaning. Better Al/Si ohmic contact.

(e) (4 points) Why do we use XeF2 to release the MEMS structure instead of using KOH?

Avoid stiction problem of wet etching when oxide beam is released.
Problem 1 continued

(f) The \(I_D\) versus \(V_G\) plot of the EE143 MOSFET [Device 8D with \(W/L = 15\mu m/10\mu m\)] is shown below. The \(V_{DS}\) bias is kept constant at 50mV.

(i) (5 points) Extract the threshold voltage from the data. Show all your calculations.

For small \(V_{DS}\) (i.e. 50mV), \(I_{DS} = \mu_n \frac{W}{L} C_{ox} (V_G - V_T) V_{DS}\)

Data has a background current of \(9.9 \times 10^{-7}\) A, the linear dependence on \(V_G\) takes off at \(V_G \sim 0.75\) volts which is \(V_T\).

(ii) (5 points) From C-V measurement, we know the gate oxide thickness 73nm. Extract the channel electron mobility \(\mu_n\) from the I-V data. Show all your calculations.

\(C_{ox} = 4.7 \times 10^{-8}\) F/cm\(^2\)

For small \(V_{DS}\) (i.e. 50mV), \(I_{DS} = \mu_n \frac{W}{L} C_{ox} (V_G - V_T) V_{DS}\)

Slope of \(I_{DS}\) versus \(V_G\) curve = \(\mu_n \frac{W}{L} C_{ox} V_{DS} \sim 5.3 \times 10^{-6}\) A/V from curve

\(\mu_n \sim \frac{5.3 \times 10^{-6}}{(15/10) \times 4.7 \times 10^{-8} \times 50 \times 10^{-3}} = 1500\) cm\(^2\)/V-sec
Problem 2 Layout (20 points total)

In the homework assignment, you have done the layout of a two-input NMOS NOR gate using poly-Si gate transistors. $V_{DD}$ is connected to the gate of T3 with Al line. The circuit diagram and conceptual layout are shown below.

(a) (5 points) What is the major advantage of the conceptual layout (shown above) in terms of layout area?

Circuit connections of the source/drains of T1, T2 and T3 are done with n+ Si (i.e. extension of the S/D regions). Since no contact holes or Al lines are used for these connections, layout area is substantially reduced.

(b) (15 points) Layout the NOR gate in the graph paper provided below if ALL transistors have the same minimum dimension of $W/L = 4 \mu m/4 \mu m$ (i.e., $2 \lambda \times 2 \lambda$).
Reference: EE143 Standard Layout symbols and Design Rules

1. Background

1.1 Lithography/etching limit on minimum feature or spacing = $2\lambda$
1.2 Alignment limit (overlay accuracy) = $\lambda$
1.3 Unless specified, default value: $\lambda = 2 \mu m$

2. Symbols and Rules

2.1 Contacts (metal to silicon)
minimum size $2\lambda \times 2\lambda$

2.2 Metal
minimum width: $2\lambda$
minimum spacing: $3\lambda$
minimum underlap of contact: $\lambda$

2.3 Polysilicon
minimum width: $2\lambda$
minimum spacing: $2\lambda$
minimum underlap of contact: $\lambda$

3. MOS Devices

3.1 Thin oxide of MOS
minimum width: $2\lambda$
minimum space: $3\lambda$
minimum underlap of contact: $\lambda$

[The thin oxide region is also known as diffusion region. The field oxide region is also called the thick oxide region]

3.2 Si Gate of MOS
Minimum gate overlap of field = $2\lambda$
Minimum contact to gate spacing = $2\lambda$
Contacts to polysilicon allowed on thick oxide only. Minimum spacing to thin oxide = $2\lambda$
Minimum poly to thin oxide spacing = $\lambda$
Problem 3 MOS Analysis (40 points total)

(a) (25 points) The following structure is a p-substrate MOS capacitor with a n+ side contact so that the inversion charge can be biased independently by a voltage supply $V_C$.

Indicate in the table below how the MOS parameters will change when the (i) gate work function $\phi_M$, (ii) substrate doping concentration $N_a$, (iii) gate oxide thickness $x_{ox}$, (iv) channel bias $V_C$, (v) Positive oxide interface charge $Q_f$ increases.

Use an ↑, ↓, or 0 to denote an increase, decrease, or no change respectively.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Voltage drop across Si substrate $V_{Si}$</th>
<th>$x_{dmax}$</th>
<th>Voltage drop across oxide $V_{ox}$</th>
<th>$V_T$</th>
<th>High-frequency small-signal capacitance $C_{min}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\phi_M$</td>
<td>↑</td>
<td>0</td>
<td>↑</td>
<td>↑</td>
<td>0</td>
</tr>
<tr>
<td>$N_a$</td>
<td>↑</td>
<td>↓</td>
<td>↑</td>
<td>↑</td>
<td>↑</td>
</tr>
<tr>
<td>$x_{ox}$</td>
<td>↑</td>
<td>0</td>
<td>↑</td>
<td>↑</td>
<td>↓</td>
</tr>
<tr>
<td>$V_C$</td>
<td>↑</td>
<td>↑</td>
<td>↑</td>
<td>↑</td>
<td>↓</td>
</tr>
<tr>
<td>$Q_f(+)$</td>
<td>↑</td>
<td>0</td>
<td>↓</td>
<td>↓</td>
<td>0</td>
</tr>
</tbody>
</table>

(b) MOSFET A and MOSFET B are both n-channel transistors. They are identical except MOSFET B has an Si/SiO2 interface charge $Q_f$.

(i) (7 points)
MOSFET A has $I_{Dsat}$ = 1 mA for $V_G$=5 volts, $V_S$= 0 volt, and $V_B$ (body bias) =0 volts. $V_T$ is known to be +0.7V.
MOSFET B has $I_{Dsat}$ = 1.5 mA for $V_G$=5 volts, $V_S$= 0 volt, and $V_B$ (body bias) =0 volts. What is the $V_T$ of MOSFET B?

$I_{Dsat} = \mu_n \frac{W}{L} C_{ox} [(V_G-V_T)^2/2]$

$1/1.5 = (5-0.7)^2 / (5-V_T(B))^2$

$V_T(B) = -0.27$ volts

(ii) (4 points) What is the corresponding $V_{Dsat}$ for MOSFET B with $V_G$=5 volts, $V_S$= 0 volt, and $V_B$ (body bias) =0 volts.

$V_{Dsat} = V_G - V_T = 5.27$ volts

(iii) (4 points) Gate oxide thickness is 100nm, calculate the oxide interface charge $Q_f$ for MOSFET B?

$\Delta V_T = 0.97$ volts = - $Q_f/C_{ox}$

$Q_f = 0.97 \times (3.45 \times 10^{-13} / 10^5) = 3.35 \times 10^{-8}$ F/cm$^2$ or $2.1 \times 10^{11}$ q/cm$^2$
Problem 4  MEMS (40 points total)

(A) The following description and figure are taken from Chapter 11 of your Jaeger textbook. Figure 11.19 depicts a process developed at the University of California at Berkeley in which the mechanical structures are formed following completion of the CMOS circuitry. A standard p-well CMOS process forms the CMOS circuitry, except for the use of tungsten metallization, which is a refractory metal that can withstand high-temperature processing. A nitride passivation layer protects the CMOS devices during MEMS machining.

The MEMS devices are fabricated over the nitride, and oxide-insulated region. Interconnection between the electromechanical devices and the active CMOS circuitry is accomplished with the polysilicon gate layer of the integrated circuit and the first polysilicon layer of the MEMS region.

(a) (5 points) Tungsten metallization is used because it can withstand high-temperature processing. What particular high-temperature processing step(s) are the description referring to? Poly-Si (P1,P2, and P3) deposition are high temperature steps (650-800 °C), Al metallization will melt if used for CMOS interconnects. Tungsten can withstand this high temperature.

(b) (5 points) Why is silicon nitride used as the passivation layer for the CMOS instead of silicon oxide? During sacrificial layer (usually oxide) etch for MEMS release, silicon nitride passivation layer will protect the CMOS area from etching.

(c) (5 points) What is the purpose of the Etch Hole shown in the MEMS structure? Etch holes allow etchant having easy access to sacrificial layer underneath, shortening lateral undercut etching time.

(d) (5 points) What is the function of the Limit Stop shown in the MEMS structure? Electrostatic deflection more than ~1/3 of gap height will collapse the beam towards the bottom. The Limit Stop can prevent excessive deflection. The Limit stop also minimize the contact area during MEMS release (stiction problem).
Problem 4  MEMS –Continuation of Part(A)

(e) (10 points) After completion of the CMOS structure processing, how many lithography steps are needed to complete fabrication of the MEMS structure? List all MEMS fabrication lithography steps AND describe their functions.

Mask 1 – contact hole opening to CMOS
P1 deposition
Mask 2- P1 patterning
Etch P1
PSG1 deposition
Mask 3 – contact hole (P2 to P1) patterning
Etch contact hole
Mask 4 – Limit stop patterning on PSG1
Etch Limit Stop feature
P2 deposition
Mask 5- P2 patterning
Etch P2
PSG2 deposition
Mask 6 – contact hole (P3 to P2) patterning
Etch contact hole
Mask 7 – Limit stop patterning on PSG2
Etch Limit Stop feature
P3 deposition
Mask 8- P3 and etch hole patterning (same mask)
Etch P3

(B) A 500 µm-thick bare Si wafer is originally flat. After a 300nm-thick oxide deposition, the wafer radius of curvature is measured to be +200 m. A 600nm nitride film is then deposited on top of the oxide and the wafer radius of curvature becomes infinity (i.e., flat, no curvature).

Calculate the stress of the nitride film alone. Is the nitride stress compressive or tensile?

(Given: ν\_Si = 0.272, E\_Si = 1.9 x 10\(^{11}\) Newton/m\(^2\))

\[
\text{RADIUS OF CURVATURE RELATIONSHIP: } \sigma_f = \frac{E_s \times t_s^2}{(1- \nu) \times 6 \times r \times t_f}
\]

With the oxide deposited, the oxide stress is compressive since \(r = +200\)m

\(t_f = 3 \times 10^{-7}\) m

\(t_s = 5 \times 10^{-4}\)m

\[
\sigma_f (\text{oxide}) = \frac{1.9 \times 10^{11} \times 25 \times 10^{-8}}{(1- 0.272) \times 6 \times 3 \times 10^{-7} \times (\text{E}_\text{Si} \times 1/\text{Si} - 1/200)} = - 1.8 \times 10^8 \text{ N/m}^2
\]

With both the nitride and the oxide deposited, \(r = \infty\), therefore \(\sigma_f (\text{oxide} + \text{nitride}) = 0\)

\[
\sigma_f (\text{nitride}) = +1.8 \times 10^8 \text{ N/m}^2 \text{ (tensile)}
\]
Problem 5 CMOS on Silicon-on-insulator (35 points total)

Design a process flow to produce the following poly-Si gate CMOS on SOI (silicon on insulator) structure. The starting material is 1µm-thick n-type single-crystalline silicon on SOI with $N_d = 2 \times 10^{15}$/cm$^3$.

(a) (10 points) List major processing advantages for CMOS on SOI as compared with CMOS on bulk Si.

Processing advantages: No Field Oxide (an channel stop implant) needed
No Well needed for NMOS and PMOS

(b) (25 points) Describe your process flow in a left column and sketch and label the cross-sections of the device after each lithography step in a right column.

The process flow is similar to a bulk CMOS process flow except no well formation and no FOX steps are needed. You have to convert one of the Si island from n-type to p-type to accommodate the NMOS.

<table>
<thead>
<tr>
<th>Process Description</th>
<th>Cross-sections</th>
</tr>
</thead>
<tbody>
<tr>
<td>Starting Material: SOI substrate</td>
<td>Si substrate</td>
</tr>
<tr>
<td><strong>The following solutions is just one of the possible solutions:</strong></td>
<td></td>
</tr>
<tr>
<td>Starting Material: n-Si on SOI (shown as Al2O3 in figures)</td>
<td></td>
</tr>
<tr>
<td>Mask#1 Define p-region opening</td>
<td></td>
</tr>
<tr>
<td>Boron implantation</td>
<td></td>
</tr>
<tr>
<td>Remove resist</td>
<td></td>
</tr>
<tr>
<td>Boron drive-in</td>
<td></td>
</tr>
<tr>
<td>Gate oxide growth</td>
<td></td>
</tr>
<tr>
<td>Undoped Poly-Si deposition by CVD</td>
<td></td>
</tr>
<tr>
<td>Mask#2 Pattern poly gates for both NMOs and PMOS</td>
<td></td>
</tr>
<tr>
<td>Mask#3 Protect PMOS regions (alignment not critical)</td>
<td>As implantation to form n+ S/D and n+ gate</td>
</tr>
<tr>
<td>---------------------------------------------------</td>
<td>-------------------------------------------</td>
</tr>
<tr>
<td><img src="image1.png" alt="Diagram" /></td>
<td><img src="image2.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Mask#4 Protect NMOS regions (alignment not critical)</th>
<th>Boron implantation to form p+ S/D and p+ gate</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image3.png" alt="Diagram" /></td>
<td><img src="image4.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Mask #5 Define isolation area which will be etched away</th>
<th>Reactive ion etching of epi Si CVD SiO₂</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image5.png" alt="Diagram" /></td>
<td><img src="image6.png" alt="Diagram" /></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Mask#6 Contact hole opening</th>
<th>Al deposition Mask#7 Al patterning</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image7.png" alt="Diagram" /></td>
<td><img src="image8.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>
Problem 6 Nonplanar Device Processing (25 points total)

You found a conceptual process flow of the DELTA (DEpleted Lean-Channel TrAnsistor) SOI MOSFET in a published paper. The key idea is to form a vertical Si pillar which is electrical isolated from the substrate by lateral thermal oxidation of the bottom part of the pillar. The top Si pillar is then used as the active MOSFET region.

Fabrication of this non-planar device structure is expected to be challenging for several process modules. In the table below, explain **concisely** the difficulties you expect to encounter.

<table>
<thead>
<tr>
<th>Process Module</th>
<th>Difficulties</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optical Lithography</td>
<td>Planarization of photoresist</td>
</tr>
<tr>
<td></td>
<td>Depth of focus to define gate</td>
</tr>
<tr>
<td>Reactive Ion Etching</td>
<td>Vertical sidewall of Si pillar</td>
</tr>
<tr>
<td></td>
<td>Large Selectivity needed to pattern gate</td>
</tr>
<tr>
<td>Thermal Oxidation</td>
<td>Volume change at pillar bottom can tilt Si pillar</td>
</tr>
<tr>
<td>Source and Drain Doping</td>
<td>Need large angle implant to doped Si pillar</td>
</tr>
<tr>
<td></td>
<td>sidewalls to form S/D</td>
</tr>
<tr>
<td>[ How to form LDD?]</td>
<td></td>
</tr>
<tr>
<td>Metal Contact to Source and Drain</td>
<td>Conformal metal deposition on S/D and planarization</td>
</tr>
</tbody>
</table>