Problem 1

(a) \( \varepsilon_f = (\alpha_f - \alpha_s) \Delta T = (24.6 - 2.6) \times 10^{-6} \times 100 = 2.2 \times 10^{-3} \)

\( \sigma_f = E_f \times \varepsilon_f = 2.2 \times 10^{-3} \times 0.7 \times 10^{11} \text{ N/m}^2 = 1.54 \times 10^8 \text{ N/m}^2 \)

(b) \( t_f = 1 \mu m = 10^{-6} \text{ m} \)

\( t_s = 50 \mu m = 5 \times 10^{-4} \text{ m} \)

\( r = \frac{E_s \times t_s^2}{(1 - \nu) \times 6 \times \sigma_f \times t_f} = 0.7 \text{ meters} \)

Problem 2

\( \sigma_f = \frac{E_s \times t_s^2}{(1 - \nu) \times 6 \times r \times t_f} \)

(a) With the oxide deposited, the oxide stress is compressive since \( r \) changes from 300m to 200m (Si wafer more curved)

\( t_f = 3 \times 10^{-7} \text{ m} \)

\( t_s = 5 \times 10^{-4} \text{ m} \)

\( \sigma_f \text{ (oxide)} = \frac{1.9 \times 10^{11} \times 25 \times 10^{-8}}{(1 - 0.272) \times 6 \times 3 \times 10^{-7} \times \left( \frac{1}{300} - \frac{1}{200} \right)} = -6.05 \times 10^7 \text{ N/m}^2 \)

(b) With both the nitride and the oxide deposited, the wafer is less curved than with oxide alone. Therefore, the nitride film has a tensile stress. However, the total stress of the dual films is still compressive since \( r = 240 \) m and is still smaller than the original curvature of 300 m.

Now, \( t_f \text{ (total)} = 9 \times 10^{-7} \text{ m} \)

\( \sigma_f \text{ (dual film)} = \frac{1.9 \times 10^{11} \times 25 \times 10^{-8}}{(1 - 0.272) \times 6 \times 9 \times 10^{-7} \times \left( \frac{1}{300} - \frac{1}{240} \right)} = -1.0 \times 10^7 \text{ N/m}^2 \)

The stress due to the nitride alone is \((-1.0 - (-6.05)) \times 10^7 \sim 5 \times 10^7 \text{ N/m}^2 \text{ (tensile)} \)

Problem 3

a) \( \rho = \text{applied force/unit length} = w \times t \times d \times g \) with density \( d = 2.3 \times 10^3 \text{ kg/m}^3 \)

\( Y(\text{at L}) = \frac{3 \rho L^4}{2Ew t^3} = \frac{3dgt^4}{2E t^2} = 52 \text{ nm} \)

b) \( F_o = 0.216 \frac{L}{L^2} \left( \frac{E}{d} \right)^{1/2} = 3.6 \text{ kHz} \)

c) A 1% increase in density \( d \) will increase \( Y(\text{at L}) \) by 1% and decrease \( F_o \) by 0.5%

d) The 0.52nm change in \( Y(\text{at L}) \) is difficult to measure using optical means [maybe do-able with atomic force microscopy]. It is probably easier to measure the 16Hz change of resonant frequency electrically.
**Problem 4**

(a)

(b) Downward if beam is heated because aluminum on top expands more than the Si beam.

(c) Process flow

```
1) Start with p wafer, n epi

2) Mask and do n+ implant

3) Mask and do p+ implant

4) CVD oxide (top & bottom)

5) Pattern SiOx (top)

6) Deposit SiNy (bottom)

7) Deposit & Pattern Al

8) Deposit & Pattern Pyrexide

9) Pattern bottom (SiOx / SiNy)

10) KOH etch at voltage for etch stop

11) Plasma release etch

( Mask areas that shouldn’t be etched )
```
Problem 5

This structure is a MEMS-before-CMOS process. The key idea is to etch the recessed area first, followed by typical poly MEMS process. The surface is planarized with CMP, and continued with standard CMOS process. After completion, the MEMS part is released by selectively etching of the sacrificial oxide. The following process flow is just one example. There can be several variations which can accomplish the final structure.

Starting material: n-epi on Si. Pattern MEMS area, use KOH to etch into epi Si, leaving tapered slope. CVD silicon nitride

![Diagram of n-epi and nitride layers on Si substrate]

CVD base polysilicon, pattern base poly

![Diagram of n-epi and nitride layers on Si substrate]

CVD sacrificial oxide 1, pattern contact hole to sacrificial oxide 1.

![Diagram of n-epi and nitride layers on Si substrate]

CVD mechanical poly which can also fill up contact hole. Pattern mechanical poly. CVD sacrificial oxide 2 over mechanical poly. CMP whole structure till planarized
CVD thin nitride and pattern over the n-epi and MEMS poly. This nitride is to protect Field Oxide from etching during MEMS release.

The following is an example CMOS process (variations are possible):
Pattern well, p-well implant and drive-in
Field oxidation (masking step here)
Gate oxidation
Poly gate deposition and patterning
n+ S/D implant
Protect NMOS (masking step here), p+ S/D implant for PMOS
CVD oxide. Open contact holes to CVD oxide

Metal 1 deposition and pattern Metal 1
CVD nitride layer for deposition. Pattern nitride openings.

Selectively etch sacrificial oxide in MEMS area to release poly structures.