Midterm Exam #2 will be on Nov 16 (Tue) 5:00-6:30pm, Moffitt 101. Closed book exam, 4 sheets of notes allowed. Topics of HW#6-HW#9 will be included.

**Reading Assignment**
1) Jaeger, pp.212-221
2) Summary sheet of EE143 layout rules (attached)
3) **Optional Reading in Bpspace**: “Design Rule Basics” from *Physical Design of CMOS IC Using L-Edit*, J.P. Uyemura. This general reading provides background info on why different rules are needed.

**Problem 1 MOS Transistor – a warmup exercise**

Your textbook shows the schematic layout of a MOSFET (not drawn to scale) with two contact holes for the source/drain. Use our EE143 layout design rules to do a minimum geometry layout which can accommodate two contact holes for the source and the drain.

*Given:* The transistor channel length $L = 4\lambda$ and channel width $W = 8\lambda$
Problem 2 NMOS Inverter
Layout a minimum geometry NMOS (poly-gate) inverter with the EE143 design rules in the graph paper provided. The circuit diagram and the schematic cross-section are shown below. \( V_{in} \), \( V_{out} \) and \( V_{DD} \) are the input voltage line, output voltage line, and supply voltage line respectively. All interconnects are aluminum lines.
Both transistors have \( W=4 \mu m \) (2\( \lambda \)) and \( L=4 \mu m \) (2\( \lambda \)). The poly-gate of transistor T2 is electrically connected to its drain with an aluminum line. Dash lines indicate contact cut to the poly-Si is to the...

Problem 3 NOR Gate
Use our EE143 design rules to layout a minimum-geometry two-input NMOS NOR gate using poly-Si gate transistors. \( V_{DD} \) is connected to the gate of T3 with Al line. To conserve space and to minimize the number of contact holes, the n+ diffusion regions are merged wherever possible.

**GIVEN** : T1 and T2 : \( W/L = 10 \mu m / 4 \mu m \) ; T3: \( W/L = 4 \mu m / 10 \mu m \). To get you started, an unfinished (not-to-scale) sketch of the top-view is provided. Any reasonable deviation from this sketch is acceptable. Draw the composite layout (including metal lines) and state the design rule used.
Problem 4 How design rules can be changed

The following cross-section shows a CMOS inverter fabricated with silicon-on-insulator (SOI) technology. Note that the buried oxide (SiO2) is a perfect electrical insulator. If we choose to use this technology. Explain how three of our EE143 MOS layout design rules can be changed (i.e., larger or smaller). Justify your explanations.
1. Background

1.1 Lithography/etching limit on minimum feature or spacing = $2\lambda$.
1.2 Alignment limit (overlay accuracy) = $\lambda$.
1.3 Unless specified, default value: $\lambda = 2\ \mu m$

2. Symbols and Rules

2.1 Contacts (metal to silicon)
minimum size $2\lambda \times 2\lambda$.

2.2 Metal
minimum width: $2\lambda$.
minimum spacing: $3\lambda$.
minimum underlap of contact: $\lambda$.

2.3 Polysilicon
minimum width: $2\lambda$.
minimum spacing: $2\lambda$.
minimum underlap of contact: $\lambda$.

3. MOS Devices

3.1 Thin oxide of MOS
minimum width: $2\lambda$.
minimum space: $3\lambda$.
minimum underlap of contact: $\lambda$.

[The thin oxide region is also known as diffusion region. The field oxide region is also called the thick oxide region]

3.2 Si Gate of MOS
Minimum gate overlap of field = $2\lambda$.
Minimum contact to gate spacing = $2\lambda$.
Contacts to polysilicon allowed on thick oxide only. Minimum spacing to thin oxide = $2\lambda$.
Minimum poly to thin oxide spacing = $\lambda$. 