Reading Assignment

1) EE143 Lecture Notes on Process Integration
2) Jaeger, pp.221-228 on CMOS integration
3) REPRINT on Bspace: Sections of Maly, Atlas of IC Technology – narrative description of CMOS process flows

In this homework assignment, we will practice designing process flows based on planar technology. You have to describe the process flow and to draw cross-sections of the devices at key processing steps.

Problem 1 Generic NMOS Process Flow

Draw the cross-sections of the NMOS device along the lines (i) A-A and (ii) B-B after
(a) The silicon nitride CVD deposition step
(b) The field oxide growth step
(c) RIE poly-Si gate step
(d) RIE of intermediate oxide and thermal oxide step
(e) Hydrogen annealing step.
Problem 1 process flow description

Substrate
Boron doped (100) Si
Resistivity = 20 Ω-cm

Thermal Oxidation
~100 Å pad oxide

CVD Si₃N₄
~ 0.1 um

Lithography
Pattern Field Oxide Regions

RIE removal of Nitride and pad oxide

Channel Stop Implant:
3x10¹² B/cm² 60 keV

Thermal Oxidation
~0.45 um oxide

Wet Etch Nitride and pad oxide

Ion Implant for Threshold Voltage control
8x10¹¹ B/cm² 35 keV

Thermal Oxidation
To grow 250 Å gate oxide

LPCVD Poly-Si ~ 0.35um

Source /Drain Implantation
~ 10¹⁶ As/cm² 80 keV

Lithography Poly-Si
Gate pattern

RIE Poly-Si gate

Lithography SiO2
~0.35um

Lithography
Contact Window pattern

Thermal Oxidation
Grow ~0.1 um oxide on poly-Si and source/drain

LPCVD SiO2
~0.35um

Lithography Al interconnect pattern

RIE removal of CVD oxide and thermal oxide

Sputter Deposit Al metal ~0.7um

Lithography Al interconnect pattern

RIE etch of Al metallization

Sintering at ~400°C in H₂ ambient to improve contact resistance and to reduce oxide interface charge
Problem 2 Double Poly DRAM

Design a process flow for the following double poly-Si NMOS dynamic random access memory (DRAM) element. Note that 1st poly and 2nd poly are separated a very thin layer of thermal oxide. A standard NMOS process is used with LOCOS to form the field oxide. Enter the process description under the first column and a sketch of the cross-section after critical process steps under the Second column.
Problem 3 RC Filter Integration

We would like to implement a simple RC low-pass filter in integrated form. The top view, the equivalent circuit, and the cross-section along line AB are shown below. The resistor body is lightly doped (n⁻) poly-Si and the top capacitor plate is heavily doped (n⁺) poly-Si. Cross-sections along AB after major processing steps are sketched in the right column of the table shown below. **Fill in the sequence of process steps used in the left column.**

<table>
<thead>
<tr>
<th>Process Description</th>
<th>Cross Section along AB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1) Starting wafer, p- Si</td>
<td>p-substrate (lightly doped)</td>
</tr>
</tbody>
</table>
Problem 4 Gate-Last MOSFET

After aluminum deposition, the processing temperature cannot exceed 650°C because the aluminum will melt. For example, the 900°C annealing step required to activate the implanted dopants for source/drain implants cannot be performed after aluminum deposition. With this constraint in mind, design a process flow for this self-aligned implanted source/drain MOSFET using Al as the gate material [shown as Al(level 1) in figure]. A schematic cross-section of the device is illustrated below. Describe the process flow and show the cross-sections at major processing steps.

[Hint: Use a high-temperature compatible material to form a “dummy” gate. After S/D formation, selectively remove the dummy gate and replace it with Al]
Problem 5 Sub-50nm MOSFET Process Flow

Optical lithography can only define features larger than 50nm. To fabricate MOSFETs with channel length less than 50nm, the following process description is found in a publication:

1. Fabricate oxide trench for device isolation
2. Form silicon nitride on pad-oxide films.
3. Pattern nitride/pad-oxide to smallest feature by optical lithography
4. \( n^+ \) S/D implant
5. Angle implant (tilted ~ \( \pm 45 \) degrees) to form \( n^+ \) pockets.
6. Form \( \text{TiSi}_2 \) on S/D regions
7. Deposit CVD oxide and planarize surface by CMP
8. Selectively remove nitride dummy gate
9. Deposit CVD oxide and form oxide spacer by RIE
10. Grow gate oxide by thermal oxidation
11. Poly-Si gate deposition by CVD
12. Pattern Poly-Si gate

The final device cross-section is illustrated below.

Let us start with a structure with oxide trench isolation already fabricated. Continue the process description with your interpretation of the process flow. Show the cross-sections at major processing steps.

**Process Description**

1) Starting structure (oxide trench isolation)

**Cross-section**

<table>
<thead>
<tr>
<th>SiO2</th>
<th>p-Si</th>
<th>SiO2</th>
</tr>
</thead>
</table>