Lecture 12: DC Biasing & Current Source Matching

- Announcements:
  - None
- Lecture Topics:
  - Aside: Getting the DC Operating Point
  - Current Source Matching Considerations
  - Op Amp Review
  - Emitter Coupled Pair (ECP)

Last Time:

\[ V_{DD} \]

\[ I_1 \rightarrow I_2 \] via \[ M_1 \] and \[ V_{GS1} = 2V_{ov} \]

\[ V_{in} \] via \[ M_2 \] and \[ V_{GS2} \]

\[ I_{D1} = I_{D2} \]

\[ \frac{1}{2} \mu n C_x \left( \frac{W}{L} \right)_1 \left( V_{DD} \right)^2 = \frac{1}{2} \mu n C \left( \frac{W}{L} \right)_3 \left( V_{ov3} \right)^2 \]

\[ \therefore \left( \frac{W}{L} \right)_1 = \frac{1}{4} \left( \frac{W}{L} \right)_3 \]

Note: Still not worry about body effects

Let's design defectively ...

\[ V_{GS1} > V_T + 2V_{ov3} \]

Current Source Matching Considerations:

- In MOS, we often need matched current sources: \( I_{D1} \approx I_{D2} \)
- \( I_{D1} = \frac{1}{2} \mu n C_x \left( \frac{W}{L} \right)_1 \left( V_{GS1}, V_T \right)^2 \)
- \( I_{D2} = \frac{1}{2} \mu n C \left( \frac{W}{L} \right)_2 \left( V_{GS2}, V_T \right)^2 \)

Finite fabrication tolerances in an IC process.

These must be perfectly matched if

\( \left( \frac{W}{L} \right)_1 = \left( \frac{W}{L} \right)_2 \) \& \( V_{GS1} = V_{GS2} \)

To quantify this:

Define average \& mismatch quantities:
### Average vs. Mismatch

<table>
<thead>
<tr>
<th>Average</th>
<th>Mismatch</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_0 = \frac{1}{2} [I_{R1} + I_{R2}] )</td>
<td>( \Delta I_0 = I_{D1} - I_{D2} )</td>
</tr>
<tr>
<td>( V_{T1} = \frac{1}{2} [V_{T1} + V_{T2}] )</td>
<td>( \Delta V_{T} = V_{T1} - V_{T2} )</td>
</tr>
</tbody>
</table>

\( \frac{\Delta I_0}{I_0} \) = fractional current mismatch

\( \frac{\Delta (W/L)}{(W/L)} \) = fractional (W/L) mismatch

\[ \frac{\Delta V_{T}}{V_{T}} \]

### Rectangularity

\( I_{D1} = I_{D} + \frac{\Delta I_{D}}{2} \)

\( I_{D2} = I_{D} - \frac{\Delta I_{D}}{2} \)

\( \frac{\Delta I_{D}}{I_{D}} = \frac{\Delta (W/L)}{(W/L)} = \frac{\Delta V_{T}}{V_{T}} \)

### Circuit Analysis

Plug these into the current equation:

\[ I_{D1} = I_{D} + \frac{\Delta I_{D}}{2} \]

\[ I_{D2} = I_{D} - \frac{\Delta I_{D}}{2} \]

\[ \frac{\Delta I_{D}}{I_{D}} = \frac{\Delta (W/L)}{(W/L)} \]

\[ \frac{\Delta V_{T}}{V_{T}} \]

This could be C- so this term doesn’t necessarily have to be.

Incorporate i.e., set curve (i.e., layout) & Current Mismatch & Index. & Bias pt.
Geffrye & DC Operating Pt.

Find $V_{BE}$: DC output voltage

Key: Find a $R$ with a well-defined voltage across it.

Well-defined voltages: $V_{CE} = 10V$, 5th, $V_{BE(on)}$

What is $V_{BE(on)} = 0.6V$ or 0.7V? Who cares?

Cannot assume $V_{BE(on)} = 0.7V$ for a forward active transistor if not forward-active.

$I_C = I_{Ref} \exp \left( \frac{V_{BE}}{V_T} \right)$

$V_{CE(on)} 
\begin{cases} 
0.7V & \text{well defined} \\
0.7V & \text{not well defined} 
\end{cases}$

$I_{Ref} = \frac{V_{CE} - V_{BE(on)}}{R_{Ref}}$

$V_{BE} = V_{BE(on)} + I_{Ref} \cdot R_{E5}$

$V_{BE} = V_{BE} + V_{BE(on)} + I_{Ref} \cdot R_{E5}$

$V_{BE} = 2V_{BE(on)} + I_{Ref} \cdot (R_{E5} + R_{E8})$

$V_{CE} = 10V$

$R_{Ref} = 10k\Omega$

$Q_1: V_{BE(on)} = 0.7V$

$Q_2: V_{BE(on)} = 0.7V$

$Q_3, Q_4: V_{BE(on)} = 0.7V$

$Q_5: V_{BE(on)} = 0.7V$

$Q_6: V_{BE(on)} = 0.7V$

$Q_7: V_{BE(on)} = 0.7V$

$Q_8: V_{BE(on)} = 0.7V$
Start Op Amps

- Ideal op amps
- Diff pairs
- Offset Voltage, Vos
- Finite Gain
- 2 stage op amps
- Finite BW
- Stability
- Compensation of Op Amps
- Slew Rate
- Power Supply Rejection
- Settling time
- Single-stage cascade op amps for better bandwidth performance

Some of the above is review

- We will do the review material using pre-made lecture notes
- Slow down for things are new to you
Ideal Op Amps

Ideal Voltage Amplifier

- ideal when \( \frac{V_s}{V_o} = A_{in} \); i.e., when source and load resistances do not influence the gain of the amplifier.

For this to occur, the voltage division at the input + output must be eliminated.

This happens when:

- \( R_s \to \infty \)
- \( R_o = 0 \)

These resistance values define an ideal voltage amplifier.

We'll look at other amplifier types later.

This then, naturally leads us to:

Ideal Operational Amplifiers (Op Amps)

- the workhorse of analog electronics -
- combination of op amps and feedback components allow the implementation of analog computers, sampled-data systems, analog filters, A/D Converters, D/A Converters, instrumentation amplifiers

In general, have a minimum of 5 terminals:

Input
- Inverting
- Non-Inverting

\[ \text{Input} \begin{cases} V^+ \vspace{0.5em} \text{Non-Inverting} \\ V^- \end{cases} \quad \text{Output} \begin{cases} V_+ \vspace{0.5em} \text{Inverting} \\ V_- \end{cases} \]

Simplify

\[ V_+ \quad V_- \quad N_o \]

Perhaps the best way to define an op amp is thru its equivalent circuit:

Equivalent Circ. of an Ideal Op Amp:

\[ N_0 = A(N_s - N_c) \]

Voltage-Controlled Voltage Source (VCVS)