Lecture 24: Slew Rate (revisited), Settling Time, and Power Supply Rejection Ratio

- Announcements:
  - HW#10 due Wednesday at 8 a.m.
  - Lab#3 (Design Project) due Friday, Dec. 11, at 11:59 p.m.
  - I'm on travel, so this is a videotape lecture
- Lecture Topics:
  - Slew Rate (revisited)
  - Settling Time
  - Power Supply Rejection Ratio (PSRR)
- Last Time:
  - Started 2nd pass at Slew Rate
  - Continue this now

Using Laplace Transform:

\( \frac{V_{A}(s)}{V_{i}(s)} = \frac{1}{1 + \frac{s}{\tau}} \)

\( \tau = \frac{1}{\omega} \)

Single (dominant) pole

\( V_{D}(s) = \frac{V_{A}}{s(1+\frac{s}{\tau})} = \frac{V_{D}}{s} - \frac{V_{D}}{s+\frac{1}{\tau}} \)

Invert Laplace transform:

\( V_{D}(t) = V_{A}(1 - e^{-t/\tau}) \) ← expected response

\( \frac{V_{D}}{V_{i}} \) [dB]

Open loop op amp

Closed loop unity gain, cut off

Theoretical Expectation

\( V_{D}(t) \)

Slope is the loop open

Reality vs. Why?
Reason it is 2nd stage of op amp cannot source enough current to mimic the shape (a quad) of a fast rising input signal.

\[ S.R.: \text{Slow Rate } \frac{dV_o}{dt} = \frac{2I_1}{C_c} \]

Example: If apply a very fast (i.e., high freq, large amplitude) sinusoid:

\[ V(t) \]

\[ \text{op amp can follow} \]

In terms of design variables:

\[ S.R. = \frac{dV_o}{dt} = \frac{I_{in}m}{C_c} = \frac{I_{in}m}{G_{m1}} \]

\[ C_c = \frac{G_{m1}}{W_{ult}A_o} \quad \text{closed-loop gain} \]

\[ W_{ult} = W@|\omega(jw)| \leq 1 \]

To Increase S.R.:

1. Decrease \( G_{m1} \) — transconductance of 1st stage
2. Increase \( W_{ult} \) — increase \( \omega_2 \) limited by the Xinput freq. range
3. Use a large \( A_o \), if possible. (only if permitted by the application)
Increasing S.R. Via $G_m$ Reduction

1. Emitter or Source Degeneration of the Input Stage

\[ \text{SR: } \frac{2I_1}{G_m} \text{, } I_1 \text{ remains the same} \]

\[ \text{Im} \cdot \frac{1}{1+g_m RE} \rightarrow \text{SR} \]

Limitations:
1. $R_e$ mismatch $\rightarrow V_{os}$
   $I_m$ must limit $V_{RE}$ to limit $V_{os}$
2. $R_e$ $\rightarrow$ gain $\downarrow$ (SR-gain trade-off)
3. $R_e$ contributes thermal noise $\rightarrow$ must limit to preserve the noise performance of the op amp.

(2) FET Input Devices

\[ S \approx \frac{g_m}{2} \]

\[ V_{os} \approx 0.2V \]

\[ \frac{V_{os}}{V_T} \approx 26 \text{mV} \]

FET S.R.

\[ \frac{I_D}{g_m} \approx \frac{1}{V_T} \]

Limitations:
1. Higher $V_{os}$
2. Increased voltage noise (but decreased current noise.)
Obtain expressions for:

1. Gain-Shunt 
2. Settling Time, $T_s$

as functions of phase margin, $\phi_m$

- Go through settling time handout

**Power Supply Rejection Ratio (PSRR)**

In today's mixed-signal ckt:

- For analog ckt, supply noise can be a big issue!
- But for analog ckt, supply noise is not much of a problem for the digital ckt.

Ex. CMOS Differential Input Stage w Current Limit Load

For this example, $PSRR = \frac{g_m V_{os}}{V_{dd}}$.
Definition: Power Supply Rejection Ratio (PSRR)

$$\text{PSRR} = \frac{\text{Gain of Input to Output}}{\text{Gain of Supply to Output}} \frac{\text{Add}v_i = 0}{\text{Add}v_i = 0}$$

For more complicated cts., much more work is req'd.

To make it easier, use a unity gain configuration. Can also get PSRR = f(ω)

$$v_{os} + v_{dd}$$

$$v_{os} + v_{dd}$$

$$v_{os} + v_{dd}$$

$$v_{os} + v_{dd}$$

$$v_{os} + v_{dd}$$

$$v_{os} + v_{dd}$$

Just find this Xform on to get PSRR+

When op amp is 1st in unity gain!
PSRR⁺ = \frac{A_{V0}^+ \left[ (1 + \frac{s}{GB})(1 + \frac{s}{PB_1}) \right]}{1 + \frac{s}{GB/A_{V0}^+}}

\text{where } GB = \text{Gain BW product} = \frac{Gm_{1}'}{C_C}
A_{V0}^+ = \text{DC PSRR⁺} = \frac{Gm_{1}'}{G_{1}G_{ds6}}

| PB₁ | \frac{Gm_{1}'}{C_{\Pi}} \text{ and } \omega⁺ = \frac{GB}{A_{V0}^+}

\text{To maximize PSRR⁺: (at dc) decrease } G_{ds6}, \text{ raise } G_{m_{1}'}

PSRR⁻ = \frac{A_{V0}^- \left[ (1 + \frac{s}{GB})(1 + \frac{s}{PB_1}) \right]}{1 + \frac{s}{GB/PB_-}}

\text{where } A_{V0}^- = \frac{Gm_{1}G_{mII}}{G_{1}G_{ds6}}
GB = \frac{Gm_{1}'}{C_C} \text{ and } \omega⁻ = \frac{C_{\Pi}}{C_{C} + C_{\Pi}} = \frac{C_{F}}{C_{C}}

| PB₁ | \frac{Gm_{1}'}{C_{\Pi}}

\text{To maximize PSRR⁻:} ① \text{decrease } G_{ds7} \\
② \text{increase } G_{mII} = G_{m6}

\text{Remarks:}
① Since often } g_{m1} < g_{m6} \Rightarrow \text{often PSRR⁻ > PSRR⁺ (at dc)}
② \omega⁻ = \frac{\omega_{p}}{\omega_{p}^-} = \frac{G_{mII}}{G_{m6}} \Rightarrow \text{that's quite loose}
\omega_{p}^- < \omega_{p}^+

\text{Thus, for an NMOS input op amp, PSRR⁻ is often better than PSRR⁺. In design, need to worry more about PSRR⁺!}

③ Some methods for \text{improving PSRR:}
(i) \text{Use buffer-based zero cancellation in the compensation loop.}
(ii) \text{Use cascode circuitry or balanced circuit topologies.}
(iii) \text{Supply-independent biasing.}
(iv) \text{Design strategies to minimize parasitic capacitive feedthrough.}