* Current sources for DC biasing and active loads:

Consider a BJT Emitter Follower:

How to generate bias voltage \( V_{be} \)?

One possibility: Resistive Divider

\[
V_{be} = \frac{V_{cc}}{R_1 + R_2} \quad V_{o}
\]

\[
R_1 = \frac{V_{be}}{I_{be}}
\]

\[
R_2 = \frac{V_{cc} - V_{be}}{I_{be}}
\]

But, with resistor variations, \( V_{be} \) may vary from ideal desired value. \( I_2 \) is very sensitive to \( V_{be} \).

How much for \( 10\% \) variation?

\[
10I_2 = I_2 = 0.1V_{be}/V_{cc} \quad I_2 = 10e\quad V_{be}/\text{Vt}
\]

\[
\Rightarrow (V_{be2} - V_{be1}) = \Delta V_{be} = V_{t}\ln(10) = \boxed{60\text{mV}}
\]

\[
\Rightarrow 10 \times \text{current error for every } 60 \text{ mV of } V_{be} \text{ error!}
\]

* \( V_{be} \) is a precision voltage \( \Rightarrow \) This is a bad design!!

* Basic principle of precision design = **Replication**

  Use same (i.e., ideally identical) device types.

  Exploit very good matching accuracy on I\(_{Q}\)s

  So, use an npn identical to \( Q_2 \) to generate \( V_{be} \).

  \[
  I_{ref} \quad V_{cc} \quad Q_1 \quad V_o
  \]

  \[
  Q_3 \quad V_{be3} = V_{be2}
  \]

  \[
  \text{Simple npn current mirror is difficult to use.}
  \]

  Note: Ideally, \( I_{ref} \) should be accurate and insensitive to Process, Voltage and Temperature (i.e., PVT) variations. This
Consider a simple NMOS current mirror:

- Let's assume $M_1$ and $M_2$ are identical in size and device parameters:
  - $M_1$ is diode connected so that $V_{DS1} = V_{GS1}$
  - Also, resistance seen by $I$ source is low as desired:
  \[ R_i = \frac{1}{g_{m1} + g_{o1}} = \frac{1}{g_{m1}} \]
  - $M_1$ always in saturation:
    \[ V_{DS} \geq (V_{GS} - V_T) \]
    \[ \text{But } V_{DS} = V_{DS} \]
    \[ V_{DS} \geq V_{DS} - V_T \text{ always true} \]

- Neglect channel-length modulation for now:
  \[ I = \frac{k}{2}(\frac{W}{L})(V_{GS} - V_T)^2 \]

  \[ V_{DS1} = \sqrt{\frac{2I}{k}} \]

  \[ I_2 = \frac{k}{2}(\frac{W}{L})(V_{GS} - V_T)^2 \]

  \[ = \frac{k}{2}(\frac{W}{L}) \left[ \sqrt{\frac{2I}{k}} - (V_T - V_T) \right] = \left(\frac{W}{L}\right)^2 \frac{I}{k} \]

- Usually design for equal $L$ values (not minimum for analog applications)

Consider some sources of error:

(2) Channel-length modulation (identical devices):

\[ I_1 = I = \frac{k}{2}(\frac{W}{L})(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

\[ I_2 = \frac{k}{2}(\frac{W}{L})(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \]

for $V_0 \geq (V_{GS} - V_T)$

\[ I_2 \neq I \quad \text{for } V_0 \neq V_{GS} \]

\[ \text{DC current offset} \]

$R_{OUT} = V_{DS}$
(c1) Consider device parameter mismatches:
\[ I_2 = \frac{K_2}{2} \left( \frac{W_2}{L_2} \right) (V_{GS} - V_{T2})^2 \left( 1 + \sqrt{1 + \frac{1}{K_2}} \right) \]
\[ I_1 = \frac{K_1}{2} \left( \frac{W_1}{L_1} \right) (V_{GS} - V_{T1})^2 \left( 1 + \sqrt{1 + \frac{1}{K_1}} \right) \]
\[ \frac{I_2}{I_1} = \frac{K_2}{K_1} \left( \frac{W_2}{W_1} \right) \left( \frac{L_1}{L_2} \right) \left( \frac{V_{GS} - V_{T2}}{V_{GS} - V_{T1}} \right)^2 \left( 1 + \sqrt{1 + \frac{1}{K_2}} \right) \left( 1 + \sqrt{1 + \frac{1}{K_1}} \right) \]

* See 3.5.6.6 - 3.5.6.7 in CM for perturbation analysis
* Make \( m_1 \neq m_2 \) identical; \( W_1 = W_2 \), \( L_1 = L_2 \), etc.

* An aside on device matching in IC's:
  * Suppose we want to match two (square) capacitors:
  * Minimum spacing set by layout rules
  * Two major effects on matching accuracy:
    1. Edge effects — Due to finite wavelength effects, etching variations, etc. Some average edge uncertainty \( \sigma_e \), which is constant and \( \neq f(L) \)
    2. Global variations (linear) across wafer; e.g. oxide thickness variation

* Side view as \( L \) increases, the difference between \( \text{Tox}_1 \) (ave) and \( \text{Tox}_2 \) (ave) increases.
So, considering edge effects and CMOS process gradients, the mismatch between ideally matched pairs looks like this:

Loft is Foundry and technology dependent. Typically, Loft is about 20 μm. Suggested Reading:


- Scaled Current copies are easy in CMOS:

```
I_{REF} \rightarrow (W/L) \rightarrow K_1 I_{REF} \rightarrow M_5 \rightarrow +V_{DD} \rightarrow M_6 \rightarrow I_{M7} \rightarrow M_7
\downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow
I_1 \quad I_2 \quad I_3 \quad I_4 \quad I_5 \quad I_6 \quad I_7
```

Current "Sinks"

Current "Sources"
(B) Consider NMOS Widlar current sources

(i) For generating small dc bias currents
(ii) For supply-independent dc bias
(iii) For process-tracking opamp frequency compensation of opamps (later)

(i) Most common Widlar configuration:

![Diagram of Widlar configuration]

- One advantage of this topology is increased Rout (i.e., it is a "better" current source than the simple one: \[ Rout = \frac{Gmz R_2 V_{OZ}}{1} \]
  improvement factor

\[ \frac{KVL}{I_0} \Rightarrow \sqrt{I_0} = -\sqrt{\frac{2}{k'(W/L)^2} + 4R_2 V_{VV} - \frac{2}{k'(W/L)^2}} \]

\[ \frac{2R_2}{R_2} \left( \frac{4}{197} \right) \]

Where \( V_{VV} = (V_{GS} - V_{TH}) = V_{DSAT} \)

- One disadvantage is back-gate effect on \( M_2 \) which is ignored in equation above

(ii) Alternative Widlar Configuration:

![Diagram of alternative Widlar configuration]

- Advantage: no backgate effect on \( M_2 \)
- Disadvantage: \( Rout = V_{OZ} \)

\[ KVL: V_{DS1} - I_1 R_1 - V_{DS2} = 0 \]

\[ \sqrt{I_0} = \sqrt{\frac{k'(W/L)^2}{2}} \left( \sqrt{\frac{2I_1}{k'(W/L)^2}} - I_1 R_1 \right) \]
(C) NPN Simple Current Mirror

\[ I_{\text{REF}} \downarrow \quad V_0 \downarrow \quad I_0 \]

- Q2 in F.A.R. for \( V_0 \geq V_{\text{SAT2}} = 0.2 \text{V} \)

- \( I_{C1} \approx I_{S1} \approx \frac{V_{BE1}}{V_T} \)

- \( V_{BE} = V_T \ln \left( \frac{I_{C1}}{I_{S1}} \right) \)

- But, \( I_{C1} \approx I_{\text{REF}} \) due to base current errors

**KCL at Q1:** \( I_{\text{REF}} = I_{C1} + I_{B1} + I_{B2} \)

Assume Q1 and Q2 are identical \( \Rightarrow I_0 = I_{C1} \)

\[ I_{\text{REF}} = I_{C1} + I_{C1} + I_{C1} \frac{I_{C1}}{V_T} = I_{C1} \left( 1 + \frac{2}{V_T} \right) \]

\[ I_{C1} = \frac{I_{\text{REF}}}{1 + \frac{2}{V_T}} \]

 Few % Error in Simple npn mirror

\( \text{in: Consider multiple scaled outputs:} \)

\[ I_{\text{REF}} \downarrow \quad 2I_{C1} \downarrow \quad Q2 \quad QN-1 \quad QN \quad V_D \quad V_B \downarrow \quad \text{IN} \downarrow \quad \text{IN}_1 \]

\[ \text{2 Identical devices} \]

**KCL at Q1:** \( I_{\text{REF}} = I_{C1} + I_{B1} + I_{B2} + I_{B3} + \ldots + I_{B_N} \)

\[ = I_{C1} + I_{C1} + I_{C1} \frac{I_{C1}}{V_T} + \ldots + I_{C1} \frac{I_{C1}}{V_T} \]

\[ = I_{C1} \left( 1 + \frac{N}{V_T} \right) \]

\[ I_{C1} = \left( \frac{I_{\text{REF}}}{1 + \frac{N}{V_T}} \right) \text{ can be large if } N \text{ is large.} \]
n-p-n current mirror with beta helper:

Idea: Take advantage of current gain of BJT to make \( I_{C1} = I_{REF} \)

\[ V_{CE1} = V_{CE2} = V_{CE} \]

\[ I_{Q1} = I_B + I_E1 \]

\[ I_{Q2} = I_B + I_E2 \]

\[ \frac{1}{\beta_2} \]

\[ KCL at Q: \]

\[ I_{REF} = I_{C1} + I_B \]

\[ = I_{Q1} + \frac{I_E2}{\beta_3+1} \]

\[ = I_{C1} + \frac{(I_B + I_B2)}{(\beta_3+1)} \]

\[ = I_{C1} + \frac{2I_C1}{\beta_1(\beta_3+1)} \]

\[ \text{so } I_{C1} = I_{REF} \]

\[ \frac{1}{1 + \frac{2}{\beta_1(\beta_3+1)}} \]

Very small error

But, be careful because \( \beta \) is not constant vs \( I \) (Fig. 1.15 6H):

\[ \beta \]

\[ \beta_0 \]

\[ \frac{\beta_0}{2} \]

\[ I_C \]

\[ 10\mu A \]

*Q1 and Q2 may operate here*

*Q3 operates here where \( \beta \) is significantly lower*
- Supply- and temperature-independent biasing:
  - As battery voltage or supply voltage changes
    - Amplifier gain changes
    - Power consumption changes
    - Amplifier bandwidth changes
    - Oscillator frequency changes
    - Similar issues as temperature changes
    - Short-term supply voltage variations
    - Power supply digital switching noise can couple into precision analog circuits.

Typical mixed-signal system:

```
VDD          
|              |
|              |
|              |
|              |
|              |
|              |

distributed
RC power grid

Digital Gate: Vin

Vout

Idd  

Ies  

Result: Power supply noise may be 100mV or more

VDD

VSS
```
General Sensitivity function:

\[ S_y = \frac{x}{y} \left( \frac{\partial y}{\partial x} \right) = \text{Sensitivity of Variable } y \text{ wrt Variable } x \]

Consider simple current source:

- Neglect base currents
- \( Q_1 \) identical to \( Q_2 \)

\[ I_0 = \frac{V_{cc}}{R} \]

\[ I_0 = \frac{V_{cc}}{R} \]

\[ \frac{\partial I_0}{\partial R} = \frac{R}{I_0} \frac{\partial I_0}{\partial R} = \frac{R}{I_0} \left( \frac{-V_{cc}}{R^2} \right) = -1 \]

This means a 20% increase in \( R \), for example, gives a -20% change in \( I_0 \) \( \rightarrow \) Bad sensitivity!

Also,

\[ \frac{\partial I_0}{\partial V_{cc}} = \frac{V_{cc}}{I_0} \frac{\partial I_0}{\partial V_{cc}} = \frac{V_{cc}}{I_0} \left( \frac{1}{R} \right) = +1 \]

\( \therefore \) Very bad supply sensitivity.

Consider Sensitivity of Widlar Current Source:

KVL: \( V_{BE1} - V_{BE2} = I_0 R_2 \)

\[ V_T \ln \frac{I_{c1}}{I_{s}} - V_T \ln \frac{I_0}{I_{s}} = I_0 R_2 \]

\[ \frac{V_T \ln I_{c1}}{I_0} = I_0 R_2 \]

\[ \text{But } I_{c1} = I_{REF} (\text{neglect base currents}) \]

\[ \therefore V_T \ln \frac{I_{REF}}{I_0} = I_0 R_2 \]

\[ \text{So, } V_T \ln \frac{I_{REF}}{I_0} = I_0 R_2 \]
\[ V_T \left[ \ln \frac{I_{RE}}{I_0} - \ln I_0 \right] = I_0 R_2 \]

Now, take derivative with respect to \( V_{CC} \):

\[ V_T \left[ \frac{1}{I_{RE}} \frac{dI_{RE}}{dV_{CC}} - \frac{1}{I_0} \frac{dI_0}{dV_{CC}} \right] = R_2 \frac{dI_0}{dV_{CC}} \]

\[ \frac{dI_0}{dV_{CC}} = \frac{V_T}{I_{RE}} \frac{dI_{RE}}{dV_{CC}} \frac{1}{R_2 + \frac{V_T}{I_0}} \]

\[ S \frac{I_0}{V_{CC}} = \frac{V_{CC}}{I_0} \frac{dI_0}{dV_{CC}} \]

\[ = \frac{V_T}{I_{RE}} \frac{dI_{RE}}{dV_{CC}} \frac{1}{R_2 + \frac{V_T}{I_0}} \]

\[ = \frac{V_T}{1 + I_0 R_2} \frac{dI_{RE}}{dV_{CC}} \]

\[ = \frac{I_0}{VT} \frac{dI_{RE}}{dV_{CC}} \]

\[ \Delta V_{BE} = 200mV \]

\[ S \frac{I_0}{V_{CC}} = \frac{1}{1 + \frac{200mV}{25mV}} = \frac{1}{9} \]

Much better than simple current mirror!!

How can we do better? Use another voltage rather than \( V_{CC} \) to generate \( I_0 \):

- \( V_{BE} \) - Base-Emitter Voltage
- \( V_T \) - MOS threshold
- Zener diode voltage
- \( V_T \) - \( VT \)
- Silicon Bandgap Voltage