Multi-stage Amplifiers with Active Loads:

(A) PMOS Current Source

Load for NMOS CS Amp:

\[ V_{DSS} = \frac{V_{DD}}{2} \]

Output Swing:

\[ V_{O} (\text{min}) = V_{\text{sat}} \]

\[ V_{O} (\text{max}) = V_{DD} - V_{\text{sat}} \]

\[ AV = -\frac{m_{2}}{g_{ds1} + g_{ds2}} \]

(B) NMOS Current Source

Load for PMOS CS Amp:

Output Swing:

\[ AV = \frac{m_{1}}{g_{ds1}} \]

\[ AV = \frac{m_{2}}{g_{ds2}} \]

But, DC level shift in pos. direction

DC level shift in neg. direction

A quick review on current sources:

I) Ideal Current Source:

\[ I = I_{D} + \frac{V}{R_{N}} \]

II) Norton Current Source:

\[ I = I_{D} + \frac{V}{R_{N}} \]

\[ I = 0 \Rightarrow V = -I_{D} R_{N} = \text{Thevin Voltage} \]

Very similar to Early Voltage, etc.

Models:

(A) NMOS

\[ R_{DS1} = \frac{V_{A1}}{I_{1}} \]

(B) PMOS

\[ R_{DS2} = \frac{V_{A2}}{I_{2}} \]
Multi-stage Amp with Active loads:
- Find: i) Input resistance; ii) Output resistance; iii) Frequency response (i.e., dominant pole freq.)

CS Stage (Replace current equivalent) M1 biased at Ib.
CD Stage (i.e., Norton active load) Sources with Norton equivalents M1 biased at Ib.

AC equivalent circuit; (low freq) at I2; m4 biased at I2.

\[ V_o = \frac{V_o}{V_i} \cdot \frac{V_o}{V_o} \cdot \frac{V_o}{V_o} \]

- \[ V_o = \frac{R_g}{R_g + R_s} \cdot V_i \]
- \[ V_o = -g_{m1} \cdot \frac{V_o}{g_{d51} + g_{d52}} \]
- \[ V_o = -g_{m1} \cdot \frac{1}{g_{d51} + g_{d52}} \]
- \[ V_o = 1 \cdot -g_{m1} \]
- \[ V_o = \frac{g_{m4}}{g_{d51} + g_{d52}} \cdot \frac{1}{1 + \eta} \] (neglect \( g_{d54} + g_{d53} \) terms)

Now, let's find the dominant pole frequency:
Now, before we apply ZVT2 method to find dominant pole frequency, let's get the capacitance to ground at nodes 0, 2 and 3: (Use Miller Effect as needed)

**Node 0:**
\[
C_0 = C_{gs1} + C_{gb1} + C_{m1} \text{ (Miller multiplied } C_{gd} \text{)}
\]
\[
C_{m1} = \frac{C_{gd} (1 - A_{Vo})}{1 + \frac{Gm1}{Gds1 + Gds2}} = \left( \frac{Gm1}{Gds1 + Gds2} \right) C_{gd}
\]
\[
\Rightarrow C_0 = C_{gs1} + C_{gb1} + C_{gd} \left( \frac{Gm1}{Gds1 + Gds2} \right)
\]

**Node 2:**
\[
C_2 = C_{x1} + C_{db1} + C_{gd2} + C_{db2} + C_{gd4} + C_{gb4} + C_{m4} \text{ (Miller multi. } C_{gs4} \text{)}
\]
\[
C_{x1} = C_{gd1} \left( 1 - \frac{1}{A_{Vo}} \right) = C_{gd1}
\]
\[
C_{m4} = C_{gs4} \left( 1 - \frac{Gm4}{Gm4 + Gm64} \right) = C_{gs4} \left( 1 - \frac{Gm4}{Gm4 + Gm64} \right)
\]
\[
= C_{gs4} \left( \frac{Gm64}{Gm4 + Gm64} \right)
\]
\[
\Rightarrow C_2 = C_{gd1} + C_{db1} + C_{gd2} + C_{db2} + C_{gd4} + C_{gb4} + C_{gs4} \left( \frac{Gm64}{Gm4 + Gm64} \right)
\]
\[
\text{ (Fairly small term)}
\]

**Node 3:**
\[
C_3 = C_{gd3} + C_{db3} + C_{sb4} + C_{x4} + C_L
\]
\[
C_{x4} = C_{gs4} \left( 1 - \frac{1}{A_{Vo4}} \right) \text{ (We will neglect negative caps)}
\]
\[
\Rightarrow C_3 = C_{gd3} + C_{db3} + C_{sb4} + C_L
\]
Now, find the driving point resistances at each node:

node 1: By inspection: \( R_1 = R_s \parallel R_{s1} \) (\( R_{s1} = \infty \))
\[ = R_s \]

node 2: By inspection: \( R_2 = \frac{1}{\frac{1}{R_{ds1}} + \frac{1}{R_{ds4}}} \) (\( R_{ds4} = \infty \))
\[ = \frac{1}{\frac{1}{R_{ds1}} + \frac{1}{R_{ds4}}} \]

node 3: By inspection: \( R_3 = \frac{1}{\frac{1}{g_{m4}} + \frac{1}{g_{m64}} + \frac{1}{g_{ds4}} + \frac{1}{g_{ds3}}} \)
\[ = \frac{1}{g_{m4} + g_{m64}} \]

\[ \therefore \text{Dominant pole} \]
\[ \omega_{3dB} = \beta_1 = \frac{1}{\frac{1}{Z_0} + \frac{1}{Z_2} + \frac{1}{Z_3}} \]
where \( Z_1 = R_0 C_0 \)
\[ Z_2 = R_2 \delta_2 \]
\[ Z_3 = R_3 \delta_3 \]

Now, let's consider a very important gain stage:

**Main Advantage:** Very high voltage gain \( E \) like two cascaded \( CS + RS \), i.e., \( AV \sim (g_{mRS})^2 \) for only one bias current, \( I \).

**Drawback:** Reduced output voltage swing; i.e., greater headroom required.
Let’s consider the output voltage swing limitations.

Observation: If we apply an input signal, $V_i$, the signal voltage at $V_o$ is large because $V_o$ is a very high impedance (i.e., high gain) node. The voltage swing at 0 and 3 are small as we will see later. So, let’s assume zero voltage signals at 0 and 3 for now.

Consider DC bias conditions:

- Must assume $V_o = V_{DD}/2$ because very high impedance node.
- Must keep $M_1-M_4$ in saturation as $V_o$ swings from $V_o$ (min) to $V_o$ (max).
- Let’s consider $M_1-M_2$ cascoded first.

* Recall: For DC bias calculations.

Use $I = \frac{k_i}{2} (\frac{W}{L}) (V_{OS} - V_f)^2$.

Note: No $V_{OS}$ So we have to assume $V_o (DC) = \frac{V_{DD}}{2}$.
\[
\begin{align*}
V_{b2} & \quad \text{①} \quad + \\
\text{V}_0 &= V_0 (\text{min}) \\
\text{V}_{ds2} & \quad \text{①} \quad + \\
\text{m}_2 & \quad - \quad \text{m}_1 \\
\text{By inspection,} \quad \text{V}_0 (\text{min}) &= \text{V}_{\text{dsat}1} + \text{V}_{\text{dsat}2} \\
\text{But, we are assuming no signal at ① so } \text{V}_{ds1} = \text{V}_{\text{dsat}1} \quad \text{is always true.}
\end{align*}
\]

- Note that cascode device, \( m_2 \), sets the DC at ①:

\[
\text{Side note: } \quad \text{V}_{ds} = V_T + (V_{gs} - V_T) = V_T + \frac{V_{ds}}{V_{dsat}}
\]

\[
\begin{align*}
\text{② } \text{V}_0 &= \text{V}_{b2} \quad \text{③} \quad \text{V}_{ds2} = \text{V}_{b2} \quad \text{V}_T - \text{V}_{\text{dsat}2} \\
\text{But, } \text{V}_0 &= \text{V}_{\text{dsat}1} \\
\Rightarrow \quad \text{V}_{b2} &= \text{V}_T + \text{V}_{\text{dsat}2} + \text{V}_{\text{dsat}1} \\
\text{Design } \text{V}_{b2} \quad \text{for} \quad \text{V}_{\text{our (min)}} &= 2 \text{V}_{\text{dsat}}
\end{align*}
\]

- Now, consider the M3-M4 PMOS cascode:

\[
\begin{align*}
\text{④ } \text{V}_{b4} & \quad \text{③} \quad \text{V}_{ds4} = \text{V}_{b4} \quad \text{V}_T - \text{V}_{\text{dsat}1} - \text{V}_{\text{dsat}4} \\
\text{By inspection,} \quad \text{V}_0 (\text{max}) &= \text{V}_{b4} - \text{\mid V}_{\text{dsat1}} - \text{\mid V}_{\text{dsat4}} \\
\text{Again, assume no voltage swing at node ③:}
\end{align*}
\]

- Note that M3 sets DC bias voltage at ③:

\[
\begin{align*}
\Rightarrow \quad \text{V}_3 &= \text{V}_{b3} + \text{V}_{gs3} = \text{V}_{b3} + \text{V}_T + \text{V}_{\text{dsat3}} \\
\text{But, we also want } \text{\mid V}_{ds4} = \text{\mid V}_{\text{dsat1}} \\
\text{So, solving as before: } \text{V}_{b3} &= \text{V}_{b0} - 12 \text{V}_{\text{dsat}}
\end{align*}
\]

- These DC designs for \( V_{b2} \) and \( V_{b3} \) are non-trivial!!
New, let's find:

- (i) Input resistance; (ii) output resistance; (iii) voltage gain and (iv) freq. response

\[
\begin{align*}
\text{(i) } R_i &= R_s + R_{g1} = R_s + 0 = R_s \\
\text{(ii) } R_o &= R_{on} \parallel R_{op}
\end{align*}
\]

Recall this circuit:

- S.S. Analysis yields:

\[
R_{on} = \frac{1 + (g_{m2} + g_{mb2} + \frac{V_o}{R_o}) R_{o1}}{g_{o2} (g_{m2} + g_{mb2} + \frac{V_o}{R_o}) R_{o1}}
\]

So, \( R_o = R_{on} \parallel R_{op} \)

\[
\approx \frac{R_{o1} (g_{m2} R_{o2})}{R_{o1} (g_{m3} R_{o3})}
\]

\( \Rightarrow R_o \) is very large impedance!

- Let's do one more new circuit:

S.S. Analysis yields:

\[
R_{s2} = \frac{1 + \frac{g_{o2} R}{g_{m2} + g_{mb2} + \frac{V_o}{R_o}}}{g_{m2} + g_{mb2} + \frac{V_o}{R_o}}
\]

Limiting cases:

- (i) \( R = 0 \) \( \Rightarrow R_{s2} = \frac{1}{g_{m2} + g_{mb2} + \frac{V_o}{R_o}} \) (familiar case)
- (ii) \( R = \frac{V_o}{N} \) (Assume \( V_o = V_{o2} \) for simplicity)

\[
\Rightarrow R_{s2} = \frac{1 + \frac{g_{o2} R_{o2}}{g_{m2} + g_{mb2} + \frac{V_o}{R_o}}}{g_{m2} + g_{mb2} + \frac{V_o}{R_o}}
\]

- (iii) Let \( R = N R_o = N R_{o2} \) (for simplicity)

\[
\Rightarrow R_{s2} = \frac{1 + \frac{N g_{o2} R_{o2}}{g_{m2} + g_{mb2} + \frac{V_o}{R_o}}}{g_{m2} + g_{mb2} + \frac{V_o}{R_o}}
\]
Now, let's compute \( Av = \frac{V_o}{V_i} \):

\[
\begin{align*}
    V_o &= (g_m R_2) V_i \\
    R_{op} &= (g_m R_2) \text{ (generated by M1 is } g_m V_i) \\
    \text{But, not all of that current flows through the high impedance output node because of current division between } R_{oi} \text{ and } R_s. \text{ This effect is often misunderstood and usually ignored, but it can be significant. From above:}
    \Rightarrow R_s &= \frac{1 + g_o R_{op}}{g_m + g_{m2} + g_o} \quad \text{(Simplify: all } g_{m1} = g_m, g_{m2} = g_{m1}, g_{m1} = g_{m1}, g_{o1} = g_o, \text{ etc.)}
    \Rightarrow R_s &= \frac{1 + g_o g_m R_o^2}{g_m + g_{m1} + g_o} = R_o \quad \text{Thus, only half of } g_m V_i \text{ flows upwards into } M_2:
    \text{Now, by inspection:}
    Av &= -\frac{1}{2} g_m R_o = -\frac{1}{2} g_m \left[ \frac{1}{R_{o1}} \left( g_{m2} R_o \right) \right] \left( g_{m3} R_o \right) \]
    \[
    = -\frac{1}{2} g_m \left[ \frac{1}{2} g_m R_o^2 \right] = -\frac{1}{4} \left( g_m R_o \right)^2
    \text{Very large gain.}
    \text{Thus, } Av \text{ of cascade gain stage is similar to that of two simple CS stages connected in cascade (i.e., in series).}
Now, freq. response starting with dominant pole:

\[ \omega_{-3dB} = \frac{1}{\frac{1}{\omega_0} + \frac{1}{\omega_2} + \frac{1}{\omega_3} + \frac{1}{\omega_4}} \]

Before we do all of these computations, let's inspect to see if we need to:

- **Node 0**: Driving point resistance
  \[ R_0 = R_S \] (probably small)

- **Node 2**: Based on our previous analysis
  \[ R_2 = \frac{R_0}{2} \] (medium value)

- **Node 4**: Same analysis as at node 2
  \[ R_4 = \frac{R_2}{2} \]

- **Node 3**: Rep \( V_{on} = R_3 = \frac{g_m R_2 R_1}{1 + g_m R_3 R_4} = \frac{R_0}{2} (g_m R_2) \) Very large driving pt. resistance.

* Note also that \( C_L \) is usually larger than the transistor capacitances. Hence,

\[ \omega_{-3dB} = \frac{1}{\frac{1}{\omega_3}} \]

\[ \omega_3 = \left[ \frac{(g_{m2} R_{d2} Y_{01})}{1 + (g_{m3} R_{d3} Y_{04})} \right] \left[ C_{gde} + C_{dib2} + C_{gdb3} + C_{db3} + C_L \right] \]

**Bode Plot**:\n
- **Dominant pole**
  \[ \omega_1 = \frac{1}{\omega_3} \]

- **(First non-dominant pole at least \( g_m R_2 \) beyond dominant pole)**
• Now, near $P_2$, $C_L$ represents a low impedance. Example: let $g_m v_o = 100$

$$v_o = \frac{1}{2} (g_m v_o) v_o = \frac{1}{2} (100) (1mA) = 50 mA$$

$$Z_0 \text{ at low freqs} = R_p \parallel R_v$$

$$Z_0 \approx \frac{1}{g_m C_L} \text{ at } \omega = 10^8 \text{ rad/sec with } C_L = 5 \mu F$$

$$\therefore Z_0 \approx 2 k \Omega \quad \text{— Now, } V_o \text{ very low impedance.}$$

• Compared to $R_p$, $1/2$ is very small at $P_2$.

Thus, we can analyze the following circuit to get $P_2$,

Because of low impedance at $V_o$:

$$v_o = \frac{1}{g_m} \text{ (now signal current)} \approx \frac{1}{g_m}$$

$$\therefore \frac{v_o}{V_o} = \frac{1}{g_m}$$

$$\therefore \frac{v_o}{V_o} = \frac{g_m}{g_m + g_m b + g_s v_s + C b}$$

$$\therefore P_2 = P_2 = \frac{2 g_m}{2 g_m + C b + g_s v_s + C b}$$

• First non-dominant pole. (See bode plot on previous page)

$$\frac{V_o}{V_0} = \frac{-g_m}{g_m} = \frac{-g_m}{g_m} = -1 \text{ V/V}$$

$$\therefore C m_0 = C x_1 = 2 C g b$$