Large-signal performance of emitter-coupled pair:

KVL:

\[ V_i - V_{be1} + V_{be2} - V_{i2} = 0 \]

\[ V_{be1} = V_T \ln \frac{I_{C1}}{I_{S1}}; \quad V_{be2} = V_T \ln \frac{I_{C2}}{I_{S2}} \]

\[ V_{id} - V_{i1} - V_{i2} - V_T \ln \frac{I_{C1}}{I_{S1}} = 0 \]

But, \( V_{id} = V_{i1} - V_{i2} \)

\[ V_{id} = V_T \ln \frac{I_{C1}}{I_{S1}} + \frac{I_{C1}}{I_{C2}} = 0 \]

Neglect \( R_{EE} \):

\[ I_{EE} = I_{C1} + I_{C2} \]

\[ I_{C1} = \frac{\alpha I_{EE}}{1 + e^{-V_{id}/V_T}} \quad \text{and} \quad I_{C2} = \frac{\alpha I_{EE}}{1 + e^{V_{id}/V_T}} \]

\[ e^{-V_{id}/V_T} = \frac{e^{-V_{id}/2V_T}}{e^{V_{id}/2V_T}} \]

\[ e^{V_{id}/V_T} = \frac{e^{V_{id}/2V_T}}{e^{-V_{id}/2V_T}} \]

\[ I_{C2} - I_{C1} = \alpha I_{EE} R_c \left[ \frac{e^{-V_{id}/2V_T}}{e^{-V_{id}/2V_T} + e^{V_{id}/2V_T}} - \frac{e^{V_{id}/2V_T}}{e^{-V_{id}/2V_T} + e^{V_{id}/2V_T}} \right] \]

\[ = \alpha I_{EE} R_c \left[ \frac{e^{-V_{id}/2V_T} - e^{V_{id}/2V_T}}{e^{-V_{id}/2V_T} + e^{V_{id}/2V_T}} \right] \]

\[ = \alpha I_{EE} R_c \left[ \frac{e^{-V_{id}/2V_T} - e^{V_{id}/2V_T}}{e^{-V_{id}/2V_T} + e^{V_{id}/2V_T}} \right] \]

\[ = \alpha I_{EE} R_c \left[ \frac{\sinh (-V_{id}/2V_T)}{\cosh (-V_{id}/2V_T)} = \alpha I_{EE} R_c \tanh \left( \frac{-V_{id}}{2V_T} \right) \right] \]

Note: \( \sinh u = \frac{1}{2} (e^u - e^{-u}) \), \( \cosh u = \frac{1}{2} (e^u + e^{-u}) \), \( u = -\frac{V_{id}}{2V_T} \)
\[ V_{od} = \alpha \cdot I_{EE} \cdot R_C \cdot \tanh \left( -\frac{V_{id}}{2V_T} \right) \]
\[ = \alpha \cdot I_{EE} \cdot R_C \left[ -\frac{V_{id}}{2V_T} + \frac{1}{3} \left( \frac{V_{id}}{2V_T} \right)^3 - \frac{1}{15} \left( \frac{V_{id}}{2V_T} \right)^5 + \ldots \right] \]

From Taylor series. Thus, \( V_{od} \) linear for small \( \frac{V_{id}}{2V_T} \).

Only linear for \(-V_T < V_{id} < V_T\) (i.e., \( |V_{id}| < 25\text{ mV} \))

- Use emitter-degeneration to linearize the amp:

- Low-voltage solution:
  The solution above requires \( V_{RE} \) more headroom than this.
  \( \alpha m \) Half-circuit:
  \[ \text{Adm} = \frac{-\alpha m \cdot R_C}{1 + \alpha m \cdot R_E} \]
  \[ \frac{V_{RE}}{V_T} \Rightarrow \]
  \( V_{BE} < V_T \) if \( V_{RE} \) is larger

\[ \text{VRE} = \frac{I_{EE} \cdot R_E}{2} \]

\[ \text{VBE} = \frac{I_{EE}}{2} \]
Large-signal Performance of NMOS source-coupled pair:

Assume: \( m_1 \) and \( m_2 \) identical and operate in saturation
- neglect \( \lambda \) effects

First, solve for \( V_{i1} - V_{i2} \):

\[
KVL: \quad V_{i1} - V_{gs1} + V_{gs2} - V_{i2} = 0
\]
\[
V_{gs1} = V_T + \sqrt{2 I_d / k_n (\mu n V_T)} \quad V_{gs2} = V_T + \sqrt{2 I_d / k_n' (\mu n' V_T)}
\]

So, \( V_{i1} - V_{i2} = V_{id} = \frac{\sqrt{I_{d1}} - \sqrt{I_{d2}}}{\sqrt{\frac{k_n}{\mu n} + \frac{k_n'}{\mu n'}}} \) \( \quad (1) \)

But, KCL at common-source node (neglect \( R_{ss} \)):
\[
I_{d1} + I_{d2} = I_{ss} \quad (2)
\]

Thus, \( V_{id} = \frac{\sqrt{I_{d1}} - \sqrt{I_{ss} - I_{d1}}}{\sqrt{\frac{k_n}{\mu n} + \frac{k_n'}{\mu n'}}} \) \( \quad (3) \)

Rearranging and using quadratic equation gives:
\[
I_{d1} = \frac{I_{ss}}{2} + \frac{k_n'}{4} \left( \frac{W}{L} \right) V_{id} \sqrt{\frac{4 I_{ss}}{k_n' (W/L)} - V_{id}^2}
\]

But, \( I_{d1} > \frac{I_{ss}}{2} \) when \( V_{id} > 0 \). Hence, only + solution is sensible. Thus,
\[
I_{d1} = \left\{ \begin{array}{ll}
\frac{I_{ss}}{2} + \frac{k_n'}{4} \left( \frac{W}{L} \right) V_{id} \sqrt{\frac{4 I_{ss}}{k_n' (W/L)} - V_{id}^2}
\end{array} \right.
\]

and \( I_{d2} = \frac{I_{ss}}{2} - \frac{k_n'}{4} \left( \frac{W}{L} \right) V_{id} \sqrt{\frac{4 I_{ss}}{k_n' (W/L)} - V_{id}^2} \)

- No triode operation by assumption no limitation on \( V_{id} \) is cutoff region of operation:
  - \( m_1 \) off when \( I_{d2} = I_{ss} \): \( 1 \rightarrow |V_{id}| \leq \sqrt{\frac{2 I_{ss}}{k_n' (W/L)}} \)
  - \( I_{d1} = \frac{I_{ss}}{2} \) when \( V_{id} = 0 \)

\( \Rightarrow |V_{id}| \leq \sqrt{\frac{2}{V_{ov}}} \)

Designer control w/o \( R_s \) degeneration!
mos differential pair with current mirror load:

Question: polarity of inputs?
- Count number of inversions from inputs to outputs:
  Note: Common-source stage is only basic inverting stage.
  Input $V_{i1}$: $V_0$ is inverting.
  Even number $= 2$ $\Rightarrow$ $V_{i1}$ is ($+$) input
  Input $V_{i2}$: $V_{0B}$ is inverting. Odd number $= 1$
  $\therefore$ $V_{i2}$ is ($-$) input

How does this stage operate? Consider DM inputs:

$V_{i1} = \frac{V_{i1}}{2}$

$0 = \frac{V_{i1}}{2}$

$V_{i2} = \frac{V_{i2}}{2}$

$0 = \frac{V_{i2}}{2}$

\[ id1 = \frac{g_m}{m} \frac{V_{i1}}{2} = g_m \frac{V_{i1}}{2} \]

\[ id2 = g_m \frac{V_{i2}}{2} \] (note: current direction opposite for negative sign)

But, $m3-m4$ mirror $id1$ into $V_0$ node as shown.

$\therefore V_0 = (id1 + id2) \cdot R_0$

$\therefore$ Full DM gain is realized! $= g_m \cdot R_0 \cdot V_{i1}$ $\therefore$ $\text{Adm} = g_m R_0$

Find $R_0$ by inspection:

$R_0 = \frac{R_D}{R_D} + \frac{1}{R_D} = \frac{R_D + 1}{R_D}$

$R_D = \frac{R_D}{1 + g_m m_2} \approx 2 \cdot R_D$

This is wrong! Why?
• There is feedback in this circuit. Inspection method usually fails when there is feedback.

• Let's find $R_o$ using feedback:

\[
l_4 = \frac{V_{\text{test}}}{V_{D4}}
\]

\[
l_2 = \frac{V_{\text{test}}}{2V_{D2}}
\]

But, $i_2$ is mirrored to the output node as shown. $i_{2m} = i_2 = \frac{V_{\text{test}}}{2V_{D2}}$

\[
I_{\text{test}} = V_{\text{test}} \left( \frac{1}{V_{D4}} + \frac{1}{2V_{D2}} + \frac{1}{2V_{D2}} \right) = V_{\text{test}} \left( \frac{1}{V_{D4}} + \frac{1}{V_{D2}} \right)
\]

• Correct answer but understand where it came from.

• Common-mode Performance:

\[
V_{ic} = \frac{V_{ic} \text{ (max)}}{CMR^+ (m1 \text{ tristate);}}
\]  

\[
V_{DD} - V_{SS} - V_{V1} + V_{V2} = V_{ic} \text{ (max)}
\]

\[
V_{ic} \text{ (max)} = V_{DD} - V_{V0} \text{ (Equal V1, V2)}
\]

\[
V_{ic} \text{ (min)} = CMR^+ (m5 \text{ tristate;})
\]

\[
V_{ic} \text{ (min)} = V_{V5} - V_{V0} - V_{SS} = 0
\]

\[
V_{ic} \text{ (min)} = V_{SS} + V_{T} - 2V_{V0}
\]
Note: NMOS pair CMR⁺ close to VDD (e.g., VDD - 0.1V) but CMR⁻ not close to VSS (e.g., VSS + 0.7V). P-MOS pair has opposite CMR range performance.

When full CM range is required, use P-MOS and N-MOS pairs in parallel. Tricky designs!

**Common-mode gain analysis:**

- Assume matched pairs

\[ I_{D1} = I_{D2} = \frac{I_{SS}}{2} \]

Key observation:

\[ I_{D1} = I_{D2} \Rightarrow V_{SD3} = V_{SD4} \]

Thus, we can analyze by shorting as shown below:

This is just a degenerated CS Amp.
By inspection: (Neglect $R_o$, which is large compared to diode-connected $m_3$ and $m_4$):

\[ G_m = \frac{g_{m1} + g_{m2}}{1 + (g_{m1} + g_{m2})V_{os}} = \frac{2g_{m1}}{1 + 2g_{m1}V_{os}} \]

\[ A_c_m = G_m R_o = \frac{2g_{m1}}{1 + 2g_{m1}V_{os}} \cdot \frac{1}{g_{m3} + g_{os} + g_{m4} + g_{os}} \]

\[ = \frac{1}{1 + 2g_{m1}V_{os}} \cdot \frac{1}{2g_{m1}V_{os}} \quad \text{(For } g_{m1} = g_{m3}, \quad 2g_{m1}V_{os} \gg 1, \quad \text{etc.}) \]

- **Input offset voltage**
- Pairs of devices are mismatched due to process variations as we saw before with capacitors: Effect - outputs railed in open loop

\[ V_o = A_{cm} (v^+ - v^-) \rightarrow V_{o0} \text{ or } V_{os} \text{ with } V_{os} \]

Typical values: $V_{os}$ few mV.

How to model - input-referred so as to be able to compare to the size of the input signal.

BJT: $V_{os}$ 1-5 mV

MOS: Higher

In BJT:

\[ I_{os} = I_{B1} - I_{B2} \]

In MOS:

\[ I_{os} = 0 \]

\[ \text{Ideal opamp} \]

\[ V_{os} = \text{Voltage needed in the configuration above to set } V_o = 0 \text{ (or } V_{o0}/2 \text{ as appropriate)} \]
Vos Problems: consider Miller Integrator

Negative Feedback.

\[ V^{-} = V^{+} = \text{Vos} \]

\[ I = \frac{\text{Vos}}{R} \]

- Initial condition: Assume \( V_c = 0 \)

\[ V_0 = \text{Vos} \]

\[ V_0 = V_{os} + \frac{1}{C} \int_0^t I \, dt = V_{os} + \frac{\text{Vos}}{RC} t \]

\[ \int = V_{os} (1 + \frac{t}{RC}) \]

\( V_0 \) will rail at \( \text{Vos} \) over time.

One solution: (Add feedback resistor)

\[ V_0 = \text{Vos} \left(1 + \frac{R_F}{R}\right) \]

So output does not rail due to \( \text{Vos} \).

But, \( R_F \) large so that \( C \) dominates (i.e., integrator)

So large dc offset at output.

- Precision circuits use offset cancellation techniques.
Vos of mismatched NMOS Differential Pair:

- Actual opamp with device mismatches
- Ideal = no mismatches but input equivalent Vos
  Vos arises due to mismatches in devices:
  - M1 \neq M2 - (W/L) and Vt Variations (neglect k' and x Variations)
- RD1 and RD2 mismatches
- Definition: \( V_{id} = Vos \) causes \( V_{od} = 0 \)

\[
\begin{align*}
KVL: \quad Vos & = V_{gs1} + V_{gs2} = 0 \\
& = (V_{t1} + \sqrt{2I_{d1}}} \kappa' (\frac{W}{L})_{1}) - (V_{t2} + \sqrt{2I_{d2}}} \kappa' (\frac{W}{L})_{2}) \\
& = (V_{t1} - V_{t2}) + \left( \sqrt{\frac{2I_{d1}}} \kappa' (\frac{W}{L})_{1} - \sqrt{\frac{2I_{d2}}} \kappa' (\frac{W}{L})_{2} \right)
\end{align*}
\]

- Define average and difference quantities as before:

\[
\Delta V_t = \sqrt{\frac{2(I_{d1} + I_{d2})}{\kappa' (\frac{W}{L})_{1} + \frac{\Delta (\frac{W}{L})}{2}}} - \sqrt{\frac{2(I_{d1} - I_{d2})}{\kappa' (\frac{W}{L})_{1} - \frac{\Delta (\frac{W}{L})}{2}}}
\]

Also use \( V_{od} = 0 \)

\[
\Delta I_d = \Delta R_d \quad \therefore \quad \frac{\Delta I_d}{I_d} = -\frac{\Delta R_d}{R_d}
\]

\[
Vos = \Delta V_t + \frac{1}{2} (V_{gs} - V_t) \left( \frac{-\Delta R_d}{R_d} - \frac{\Delta (\frac{W}{L})}{(\frac{W}{L})_1} \right)
\]