Today: High-Swing Current Mirrors (4.2.5.2 GM)

Motivation = High Dynamic Range (DR)

\[ \text{output} \text{(max)} = \frac{V_{out}(\text{max})}{V_{out}(\text{min})} \text{ -- Limited by distortion} \]

\[ \text{output} \text{(max)} = \frac{V_{out}(\text{min})}{V_{out}(\text{max})} \text{ -- Limited by noise} \]

Let's consider output swing versus distortion:

- **V_{DD}**
- We know \( \alpha = \frac{g_{m1}}{g_{o1} + g_{o2}} \)
- This is only true with \( M1 \) and \( M2 \) in saturation. Why saturation?

\[ E_d \]

\[ \text{Tria}(V_{gs}, V_{ds}) \]

\[ \text{SAT}(V_{gs}, V_{ds}) \]

\[ V_{gs2} \]

\[ V_{gs1} \]

\[ \text{V}_{gs} \]

\[ \text{V}_{gs1} - V_{T} \]

\[ \text{V}_{gs2} - V_{T} \]

\[ V_{o1} \]

\[ V_{o2} \]

\[ V_{o} \]

\[ V_{o}(t) \]

\[ V_{o}(t) \text{ vs. } V_{g} \]

\[ V_{o}(t) \text{ vs. } V_{g} \]

\[ \text{Linear region operation} \]

\[ \text{with a relatively small } V_{i}(t) \]

\[ \text{Note:} \]

\[ V_{out}(\text{min}) > V_{o1} \]

\[ V_{out}(\text{max}) < V_{DD} - V_{o2} \]
(ii) Relatively large input signal

- Low-gain nonlinear regions with high distortion levels.
- Example of performance degradation in this case—consider a cellphone receiver amplifier (i.e., an LNA - low-noise amplifier)

Antenna

- LNA handles small signals linearly as in (i)
- Now suppose a friend is nearby talk on his cellphone — your phone will receive this signal too. Very large because close. What happens — gain desensitization or gain compression due to blocker.

\[ \text{dBm} \]

Received signal

Band of interest

\[ V(t) \]

Effect on desired signal

Linear high-gain regions

Compressed gain

Low-gain regions
Simple current mirror bias for CS Amp:

\[ V_{B2} = V_{DD} - V_{S63} = V_{DD} - 1V_{R31} - \left( V_{S63} - 1V_{R31} \right) / V_{OV3} \]

But, \( V_{OV3} = \sqrt{\frac{2I_D}{K_P(WL)_3}} \)

Thus, \( V_0 (\text{min}) = V_{OV1} \) \( V_0 (\text{max}) = V_{DD} - V_{OV2} \{ m_2 \text{ and } m_3 \text{ are identical.} \}

Now, consider bias generators for a much better amplifier — cascade Amp

By inspection,

\[ A_v = -\frac{g_{m4}}{g_{m1} + g_{m4} / g_{m2} g_{m3} g_{m3}} \]

(very large gain)

Maintain \( M1-M4 \) in saturation over output voltage swing range.

For the best possible design:

\[ V_{DS1} = V_{OV1}; V_{DS2} (\text{min}) = V_{OV2}; V_{DS3} (\text{min}) = V_{OV3}; V_{OV4} = V_{DD} - 2V_{OV} \]

Thus, \( V_0 (\text{max}) = V_{DD} - V_{OV2} - V_{OV4} = V_{DD} - 2V_{OV} \)

\( V_0 (\text{min}) = V_{OV1} + V_{OV2} = 2V_{OV} \)

\[ V_0 \text{ (swing)} = V_0 \text{ (max)} - V_0 \text{ (min)} \]

Example: \( V_{DD} = 1.2V; V_{OV} = 100mV; V_0 \text{ (swing)} = 0.8V \).
Consider a cascode current source bias generator:

- $M_1$ and $M_5$ identical
- $M_2$ and $M_6$ identical but not necessarily same as $M_1$, $M_5$

Find DC voltage $V_\Box$:

$$V_{GS5} = V_{T5} + \frac{2I}{k_n(W/L)_5}$$

$$V_{GS6} = V_{T6} + \frac{2I}{k_n(W/L)_6} = V_{T6} + V_{OV6} \quad (V_{T6} > V_{TNO})$$

$$V_{GS2} = V_{T2} + \frac{2I}{k_n(W/L)_2} = V_{T2} + V_{OV2} \quad (V_{T2} > V_{TNO})$$

KVL: $V_\Box = V_{GS5} + V_{GS6} - V_{GS2} \quad (Assume V_{OV1} = V_{OV})$

$$= (V_{TNO} + V_{OV}) + (V_{T6} + V_{OV}) - (V_{T2} + V_{OV})$$

$$= V_{TNO} + V_{OV} + (V_{T6} - V_{T2})$$

$\therefore V_0 (min) = V_\Box + V_{OV2} = V_{TNO} + 2V_{OV}$

$V_0 (max) = V_{DD} - (V_{TPO}) - 2V_{OV} \quad (Similar \ bias \ for \ M_3)$

$\therefore V_0 (swing) = V_0 (max) - V_0 (min)$

$$= V_{DD} - (V_{TNO} + V_{TPO}) - 4V_{OV}$$

**Example:**

$V_{DD} = 1.2V$; $V_{TNO} = 0.5V$; $V_{TPO} = -0.5V$; $V_{OV} = 0.1V$

$V_0 (swing) = 1.2 - (0.5 + 0.5) - 4(0.1) = -0.2V \Rightarrow$ Not possible: Need $V_{DD} \geq 2V$ for $V_0 (swing) \geq 0V$.

**We want:** $V_0 (swing) = V_{DD} - 4V_{OV}$

$\therefore$ Get rid of two threshold voltage terms.
Conceptual Solution: Add DC Level Shifter

KVL:
\[ V_{\text{X}} = V_{655} + V_{656} - V_{\text{BAT}} - V_{652} \]
\[ = V_{TN0} + (V_{T6} - V_{T2}) + V_{0V} - V_{\text{BAT}} \]
For \( V_{\text{X}} = V_{0V} \), we need:
\[ V_{\text{BAT}} = V_{TN0} + (V_{T6} - V_{T2}) \]
(Note: \( V_{T6} > V_{T2} \) because
\[ V_{SB6} = V_{655} = V_{TN0} + V_{0V} \]
and
\[ V_{SB2} = V_{0V} \]) (Assume \( V_{T6} = V_{T2} \))

\[ V_{\text{BAT}} = V_{T0} \]

Implement using NMOS source-follower:

KCL:
\[ V_{\text{X}} = V_{655} + V_{656} \]
\[ -V_{657} - V_{652} \]
Assuming \( V_{T7} = V_{T} \)
and \( V_{0V} = V_{0V} \),
\[ V_{\text{X}} = V_{0V} \text{ means } \]
\[ V_{0V} = 0 \]

\[ V_{0V} = \frac{\sqrt{2I_{7}}}{k_{n}(W/L)_{7}} = 0 \text{ means: i) } I_{7} = 0 \]
and/or ii) \( (W/L)_{7} \) very big.

- Bad design because of weird way \( M_{7} \) is used.
- Let's consider some sensible changes to this circuit based on our basic goals:
  1. \( V_{\text{X}} = V_{0V} \)
  2. \( V_{0} \text{ (min)} = 2V_{0V} \)
Observation: With $V_{TH} = V_T, V_{IS}$ can only equal $V_{OV}$ if $V_{OS5}$ or $V_{OS6}$ equals $2V_{OV}$. Let's not mess with bottom row ($M_5, M_B, M_I$) so let's design for $V_{OV6} = 2V_{OV}$ (i.e., $V_{OV1} = V_{OV2} = V_{OV5} = V_{OV7} = V_{OV8} = V_{OV}$)

$$V_{OV6} = \sqrt{\frac{2I}{k_n(W/L)}} = 2V_{OV} \quad \Rightarrow \quad \left(\frac{W}{L}\right)_6 = \frac{2}{\sqrt{2}} \left(\frac{W}{L}\right)_{\text{for other devices}}$$

This is a practical size for $M_6$.

Body Effect Problem: (All NMOS bulks to ground)

For $M_1, M_5, M_B, V_{SB} = 0$; $V_{TH} = V_{TS} = V_{TB} = V_{TNO}$

- But, $V_{SB} \neq 0$ for $M_2, M_7$ & $M_B$:

  $V_{SB6} = V_{SB} - V_{OV} = (V_{TNO} + V_{OV}) \quad \Rightarrow \quad +\Delta V$ compared to $V_{TNO}$

  $V_{SB7} = V_{SB} - V_{OV} = (V_{TB} + 2V_{OV}) \quad \Rightarrow \quad +\Delta V$ compared to $V_{TNO}$

  $V_{SB2} = V_{SB} - V_{OV} = V_{OV} \quad \Rightarrow \quad +\Delta V$ compared to $V_{TNO}$

Recall:

$$V_{IS} = V_{GS5} + V_{GS6} - V_{GS7} - V_{GS2}$$

$$= (V_{TNO} + V_{OV}) + (V_{TB} + 2V_{OV}) - (V_{TB} + V_{OV}) - (V_{TNO} - V_{TB}) + V_{OV}$$

$$= V_{TNO - 2V_{OV}} + (V_{TB} - V_{TNO}) + V_{OV} \quad \Rightarrow \quad (V_{IS} < 0 \quad \text{for} \quad V_{SB} < 0)$$

$\therefore V_{IS} < V_{OV}$
Other problems with this circuit:

\[ V_{DS} = V_{DS1} \quad \therefore \text{Current mismatch} \]

\[ I_1 = \frac{k_n}{2} \left( \frac{1}{2} \right) (V_{DS1} - V_{TN0})^2 (1 + \lambda V_{DS1}) \]

\[ I_5 = \frac{k_n}{2} \left( \frac{1}{2} \right) (V_{DS5} - V_{TN0})^2 (1 + \lambda V_{DS5}) = I_{REF} = I \]

\[ \frac{I_1}{I_5} = \frac{1 + \lambda V_{OV}}{1 + \lambda V_{OV}} \approx (1 + \lambda V_{OV}) \left( 1 - \lambda (V_{TN0} - V_{OV}) \right) \]

\[ \approx 1 - \lambda (V_{TN0} - 2 V_{OV}) \]

- Would like \( V_{DS5} = V_{DS1} \) for higher accuracy.
- Another issue is headroom requirement:

- At the drain of \( M_6 \), \( V_{D6} = 2V_T + 3V_{OV} \)

  Example: \( V_{TN0} = 0.5V \); \( V_{OV} = 0.1V \)

  \[ V_{DD} > V_{D6} > 1.3V \]

  For modern CMOS processes: \( V_{DD} = 1.2\)V or \( V_{DD} = 0.8\)V

Solution: High-Swing Cascode Current Source

\[ V_{OV} = V_{OV} \ (\text{desired}) \]

\[ V_{B2} = V_T + 2V_{OV} \]

Note: \( V_{DS5} = V_{DS1} = V_O = V_{OV} \)

\[ \therefore \text{No systematic error in } I_D \text{ versus } I_{DS}. \]

But, \( V_{O2} \neq V_{O6} = V_{DS5} \).

This is usually not a problem because \( I_0 \) does not vary much from \( I_{D1} = I_{D5} = I \) as set by \( M_1 \) and \( M_5 \). Why is this so?