Terminal Gain and I/O Resistances of BJT Amplifiers

<table>
<thead>
<tr>
<th>Common Emitter (CE)</th>
<th>Common Collector (CC)</th>
<th>Common Base (CB)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Common Emitter Diagram" /></td>
<td><img src="image2" alt="Common Collector Diagram" /></td>
<td><img src="image3" alt="Common Base Diagram" /></td>
</tr>
<tr>
<td>( A_{v,1} = \frac{g_m R_l}{1 + g_m R_L} )</td>
<td>( A_{v,1} = \frac{R_l}{g_m + R_L} )</td>
<td>( A_{v,1} = g_m R_L \beta )</td>
</tr>
<tr>
<td>( R_i = r_e + (\beta + 1) R_L )</td>
<td>( R_i = r_e + R_{th} )</td>
<td>( R_i = \frac{1}{g_m} )</td>
</tr>
<tr>
<td>( R_o = \left[ r_e (1 + g_m R_L) \right] )</td>
<td>( R_o = \frac{1 + \beta}{g_m} + \frac{R_L}{\beta} )</td>
<td>( R_o = \left[ r_e (1 + g_m R_L) \right] )</td>
</tr>
<tr>
<td>( A_{i,1} = \beta )</td>
<td>( A_{i,1} = \beta + 1 )</td>
<td>( A_{i,1} \approx 1 )</td>
</tr>
</tbody>
</table>

For the gain, \( R_i, R_o \) of the whole amplifier, you need to include voltage/current dividers at input and output stages.
Terminal Gain and I/O Resistances of MOS Amplifiers

<table>
<thead>
<tr>
<th>Common Source (CS)</th>
<th>Common Drain (CD)</th>
<th>Common Gate (CG)</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image1" alt="Common Source" /></td>
<td><img src="image2" alt="Common Drain" /></td>
<td><img src="image3" alt="Common Gate" /></td>
</tr>
</tbody>
</table>

\[ A_{v,1} = -\frac{g_m R_L}{1 + g_m R_S} \]
\[ R_i = \infty \]
\[ R_o = \left[ r_c (1 + g_m R_S) \right] \]
\[ A_{i,1} = \infty \]

Without degeneration:
Simply set \( R_i = 0 \)

\[ A_{v,1} = \frac{R_i}{R_m + R_L} \]
\[ R_i = \infty \]
\[ R_o = \frac{1}{g_m} \]
\[ A_{i,1} = \frac{1}{g_m} \]

For the gain, \( R_i, R_o \) of the whole amplifier, you need to include voltage/current dividers at input and output stages.

Summary of Single-Transistor Amplifiers

<table>
<thead>
<tr>
<th>BJT</th>
<th>Ideal Voltage Amplifiers</th>
<th>Common Emitter</th>
<th>Common Emitter with Deg.</th>
<th>Common Collector</th>
<th>Common Base</th>
</tr>
</thead>
<tbody>
<tr>
<td>BJT</td>
<td>( R_i )</td>
<td>( \infty )</td>
<td>Moderate</td>
<td>Large</td>
<td>Large</td>
</tr>
<tr>
<td>BJT</td>
<td>( R_o )</td>
<td>0</td>
<td>Large</td>
<td>Very Large</td>
<td>Small</td>
</tr>
<tr>
<td>BJT</td>
<td>( A_{v} )</td>
<td>( \infty )</td>
<td>Large</td>
<td>Moderate</td>
<td>~ 1</td>
</tr>
<tr>
<td>BJT</td>
<td>( f_{H} )</td>
<td>( \infty )</td>
<td>Small</td>
<td>Moderate</td>
<td>Large</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MOS</th>
<th>Ideal Voltage Amplifiers</th>
<th>Common Source</th>
<th>Common Source with Deg.</th>
<th>Common Drain</th>
<th>Common Gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS</td>
<td>( R_i )</td>
<td>( \infty )</td>
<td>Very Large</td>
<td>Very Large</td>
<td>Large</td>
</tr>
<tr>
<td>MOS</td>
<td>( R_o )</td>
<td>0</td>
<td>Large</td>
<td>Very Large</td>
<td>Small</td>
</tr>
<tr>
<td>MOS</td>
<td>( A_{v} )</td>
<td>( \infty )</td>
<td>Moderate</td>
<td>Small</td>
<td>~ 1</td>
</tr>
<tr>
<td>MOS</td>
<td>( f_{H} )</td>
<td>( \infty )</td>
<td>Small</td>
<td>Moderate</td>
<td>Large</td>
</tr>
</tbody>
</table>
Need for Multistage Amplifiers

- Typical spec for a general purpose operational amplifier
  - Input resistance ~ 1MΩ
  - Output resistance ~ 100Ω
  - Voltage gain ~ 100,000
- No single transistor amplifier can satisfy the spec
- Cascading multiple stages of amplifiers to meet the spec
- Usually
  - An input stage to provide required input resistance
  - A middle stage(s) to provide gain
  - An output stage to provide required output resistance
- It is important to note that the input resistance of the follow-on stage becomes the load of the previous stage

A 3-Stage ac-coupled Amplifier Circuit

- MOSFET $M_1$ operating in the C-S configuration provides high input resistance and moderate voltage gain.
- BJT $Q_2$ in a C-E configuration, the second stage, provides high gain.
- BJT $Q_3$, an emitter-follower gives low output resistance and buffers the high gain stage from the relatively low value of load resistance.
A 3-Stage ac-coupled Amplifier Circuit

- Input and output of overall amplifier is ac-coupled through capacitors $C_1$ and $C_6$.
- Bypass capacitors $C_2$ and $C_4$ are used to get maximum voltage gain from the two inverting amplifiers.
- Interstage coupling capacitors $C_3$ and $C_5$ transfer ac signals between amplifiers but provide isolation at dc and prevent Q-points of the transistors from being affected.
- In the ac equivalent circuit, bias resistors are replaced by $R_{B2} = R_1||R_2$ and $R_{B3} = R_3||R_4$

dc Equivalent Circuit

At dc, the capacitors isolate each individual transistor stage from the others. Thus, the bias point for each transistor may be found using the single transistor analysis methods already discussed.
Input Resistance and Voltage Gain

\[ A_i = A_{i1}A_{i2}A_{i3} \frac{R_R}{R_R + R_i} \]

\[ A_{i1} = \frac{v_1}{v_3} = -g_{m1}R_{i1} = -0.015\times0.478\times0.1\times0.1 = -4.78 \]

\[ v_1 = \frac{R_R}{R_R + R_i} = v \times \frac{1M\Omega}{10M\Omega + 1M\Omega} = 0.990v_i \]

\[ R_{i2} = R_{i2} + R_{i2} + R_{i2} = 3.54\times3.54\times3.54 = 3.54\times1000 = 3540\Omega \]

\[ A_{i2} = \frac{v_2}{v_3} = -g_{m2}R_{i2} = -62.8\times3.54\times0.1\times0.1 = -222 \]

\[ A_{i3} = \frac{v_3}{v_3} = \frac{\beta_{o1}R_{i3}}{R_{i3} + (\beta_{o1} + 1)R_{i3}} = 0.950 \]

\[ A_i = A_{i1}A_{i2}A_{i3} + \frac{R_R}{R_R + R_i} = +998 \]
Output Resistance

\[ R_\text{o3} = r_\pi + R_{th1} + \beta \approx g_m + R_{th1} \]

\[ R_{th1} = R_{I2} | R_{o2}^2 = 4.3 \Omega \]

\[ R_\text{o3} = 179.6 \text{ m\Omega} + 4 \text{ k}\Omega = 61.3 \Omega \]

Current and Power Gain

The input signal current delivered to the amplifier from source \( v_1 \) is

\[ i = \frac{v_1}{R_I + R_s} = 9.90 \times 10^{-7} v_1 \]

and the signal current delivered to the load resistor is

\[ i_L = \frac{A_v v_1}{R_L} = \frac{A_v 998 v_1}{250 \Omega} = 3.99 v_1 \]

Current Gain: \( A_i = \frac{i}{i} = 4.03 \times 10^3 \) (132 dB)

Voltage Gain: \( A_v = \frac{v_o}{v_i} = 9.98 \times 10^7 \) (60 dB)

Power Gain: \( A_p = \frac{P_o}{P_i} = \frac{v_L i_L}{v_i^2} = A_i A_v = 4.02 \times 10^7 \) (96 dB)
**Input and Output Signal Range**

For the first stage:  \( |v_i| \leq 0.2(V_{GS} - V_{TH}) \) \( \Rightarrow \)  \( |v_i| \leq \frac{0.2(-1+2)V}{0.99} = 0.202 \) V

For the second stage:  \( |v_{ib}| = |v_{ib}| = |A_{iv}| \leq 5mV \)

\( |v_i| \leq \frac{5mV}{A_{iv}} = \frac{5mV}{4.78} = 1.05mV \) \( \Rightarrow \)  \( |v_i| \leq \frac{1.05mV}{0.99} = 1.06 \) mV

For the third stage:  \( v_{ib} = \frac{v_i}{1+g_{m3}R_{L3}} = \frac{A_{iv}A_{iv}(0.990V)}{1+g_{m3}R_{L3}} \)

\( |v_i| \leq \frac{1+g_{m3}R_{L3}}{A_{iv}A_{iv}(0.990)} \cdot 5mV = 92.7 \) \( \mu \)V

Overall:  \( |v_i| \leq \min(202mV, 1.06mV, 92.7\mu V) = 92.7\mu V \)

\( |v_i| \leq A_{iv}(92.7\mu V) = 998(92.7\mu V) = 92.5 \) mV

**SPICE Simulation Circuit**
SPICE Simulation Results

\[ A_v = 1000 \quad f_L = 500 \text{ Hz} \quad f_H = 500 \text{ kHz} \]

**SPICE Simulation Results**

\[ v_{in} = 100 \mu V \]

Simulation with undistorted output and gain of 1000.
SPICE Simulation Results

\[ v_{in} = 750 \, \mu V \]

Distorted output with amplitude exceeding output voltage capability of amplifier.

Short-Circuit Time Constant Estimate for \( f_L \)

An estimate for the lower cutoff frequency for an amplifier with multiple coupling and bypass capacitors is given by the sum of the reciprocals of the "short-circuit" time constants:

\[ f_L \approx \frac{1}{2\pi} \sum_{i=1}^{n} \frac{1}{R_{IS} C_i} \]

where \( R_{IS} \) is the resistance at the terminals of the \( i \)th capacitor with all the other capacitors shorted.
Short-Circuit Time Constant Estimate for $f_L$

$$\frac{1}{2\pi} \left[ \frac{1}{1.01\,\text{M}\Omega(22\,\mu\text{F})} + \frac{1}{66.7\,\Omega(22\,\mu\text{F})} + \frac{1}{2.72\,\text{k}\Omega(22\,\mu\text{F})} + \frac{1}{19.2\,\text{kHz}(22\,\mu\text{F})} 
+ \frac{1}{18.9\,\Omega(22\,\mu\text{F})} + \frac{1}{315\,\Omega(22\,\mu\text{F})} \right] = 511\,\text{Hz}$$