CS252 HOMEWORK 3

Due Tues. 11/06/07

Problem 1:

Here is some code for a vector machine with a maximum vector length of 64 elements:

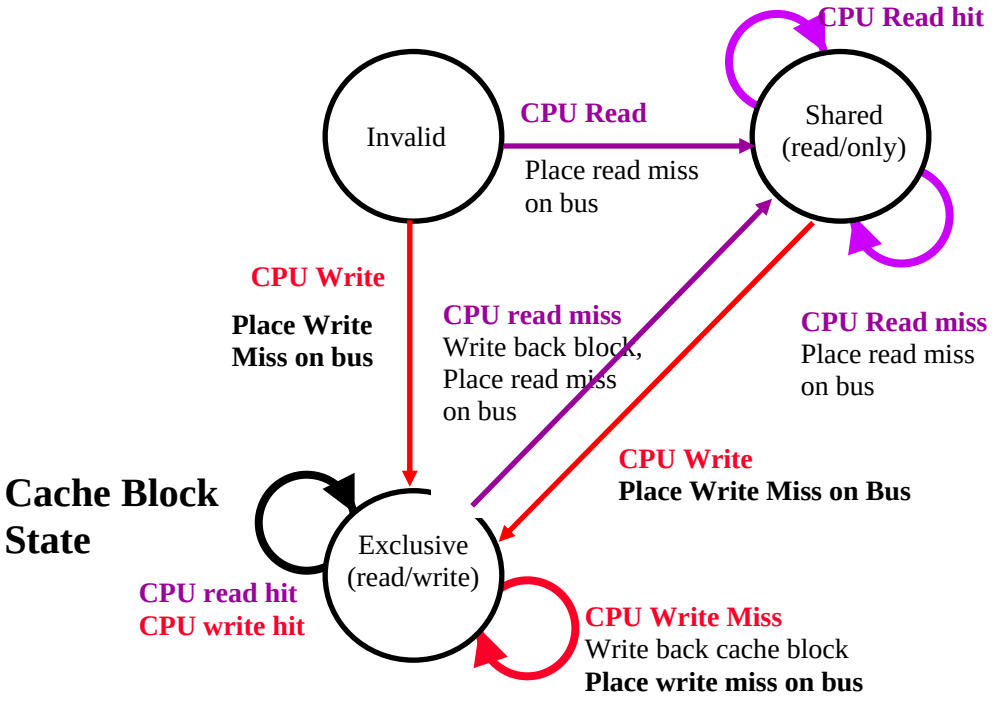
```
LP:   LV      V1, R5      # load V1 with new value
      MULTSV  V2, F0, V1  # perform the calculation
      MULTSV  V3, F1, V1
      ADDV    V2, V2, V3
      MULTSV  V4, F2, V1
      ADDV    V2, V2, V4
      SV      V2, R5      # store the result
      SUBI    R5, R5, 8
      BNEZ    R5, LP
```

a) Show the convoys in the above code. Do not worry about structural hazards; assume that there are enough functional units. (Note that when analyzing convoys you may ignore the last two instructions since those are not vector computations.)

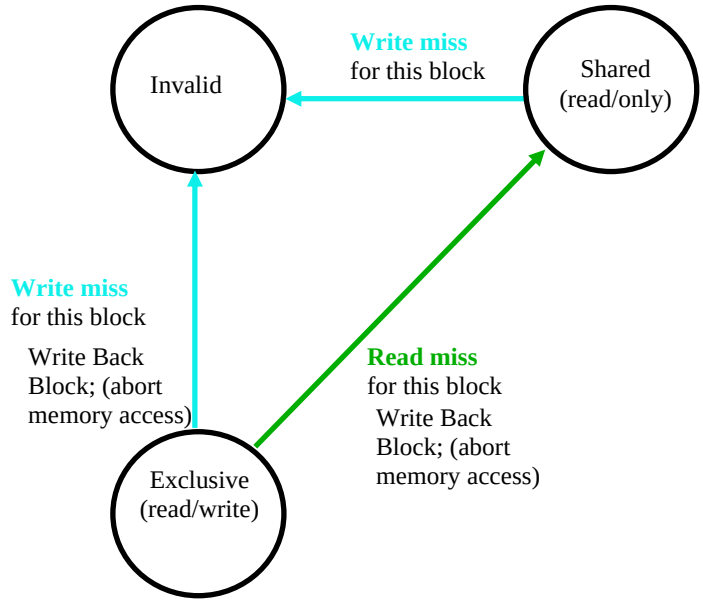
b) Show the execution time in clock cycles of this loop with n elements (T_n); assume Tloop = 15 and Tstart = 7 for all vector codes. Assume Tstart is the startup time for each convoy. Show the equation, and give the value of execution time for vector length n=64.

Problem 2:

This shows a snooping protocol state diagram for a for each cache block, based on CPU requests:



This shows a snooping protocol state diagram for each cache block, based on requests from the bus:



Assume that address A1 and A2 are different addresses that map to the same cache block. P1 and P2 are two processors that use the above snooping protocol. Complete the table below to show the actions the result when the following events occur. Extra blank lines are provided in case an event causes multiple actions; you may not need to use all the blank lines.

Event	P1 state	P1 addr	P1 val	P2 state	P2 addr	P2 val	Bus action	Bus proc	Bus addr	Bus val	Mem addr	Mem val
P1 write 5 to A1												
P2 write 1 to A2												
P2 write 2 to A1												
P1 read A1												

Problem 3:

Assume X1 and X2 are different values in the same cache block. Assume that P1 and P2 are two different processors using the snooping protocol described in problem 2. For the following events, describe if the access is a hit or a miss in the accessing processor, and if it generates invalidates in the other processor; for misses and invalidates, describe if they are true or false sharing misses (or mark not applicable). Neither P1 nor P2 has either value, to begin with.

Time	P1	P2	Hit or Miss? Invalidates?	If Miss or Invalidate, True or False sharing?
1	Write X2			
2		Write X2		
3	Read X1			
4		Read X1		
5		Write X2		
6	Read X1			