## UNIVERSITY OF CALIFORNIA

## College of Engineering Department of Electrical Engineering and Computer Sciences NTU IC-776CA

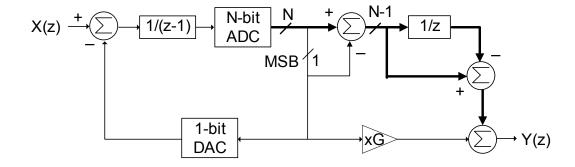
B. E. BOSER

Homework 6 Due Thursday, Mar 30, 2006 EECS 247 Spring 2006

- 1. Download the datasheet of the AD7677 A/D converter from <a href="www.analog.com">www.analog.com</a>.
- a) Using the given code histograms for DC input, calculate the converter's input referred thermal noise in LSB rms. (Follow the method presented in: S. Ruscak and L. Singer, "Using Histogram Techniques to Measure A/D Converter Noise," available at

http://www.analog.com/library/analogDialogue/archives/29-2/cnvtrnoise.html).

- b) Using the data from the typical DNL plot, estimate the expected quantization noise in LSB rms error of the converter. Assume that the DNL is distributed uniformly over the bounds seen in the DNL plot.
- c) Combine the results of a) and b) to obtain an estimate for the converter's SNR. Does this number agree with the typical value given in the data sheet?
- d) What is the ENOB of this converter?
- e) The typical low frequency DFT plot of the AD7677 shows a dominant 3<sup>rd</sup> harmonic. Use your analysis from problem 2 of homework 4 to estimate the converter's SFDR from the peak INL seen in the given typical INL plot. Does this number agree with the specified typical SFDR value?
- 2. The sigma-delta modulator below employs an N-bit ADC for increased resolution, but only a 1-bit DAC is used to avoid distortion due to DAC nonlinearity. The remaining N-1 bits of ADC outputs serve as an estimate of the quantization error.
- a) Find Y(z) as a function of the input X(z), quantization error  $E_1(z)$  and ADC truncation error  $E_2(z)$ . What is the optimal value for G in order to eliminate the truncation error in Y(z)?
- b) Compute the dynamic range of the converter as a function of N and the oversampling ratio M. Assume optimal setting of G calculated in a) and an ideal (i.e. brickwall) decimation filter.



Hint:  $E_1(z)$  and  $E_2(z)$  can be modeled as additive white noise sources. As a result the system can be modeled as a linearized schematic as following. Note that an ideal DAC doesn't introduce any error.

